

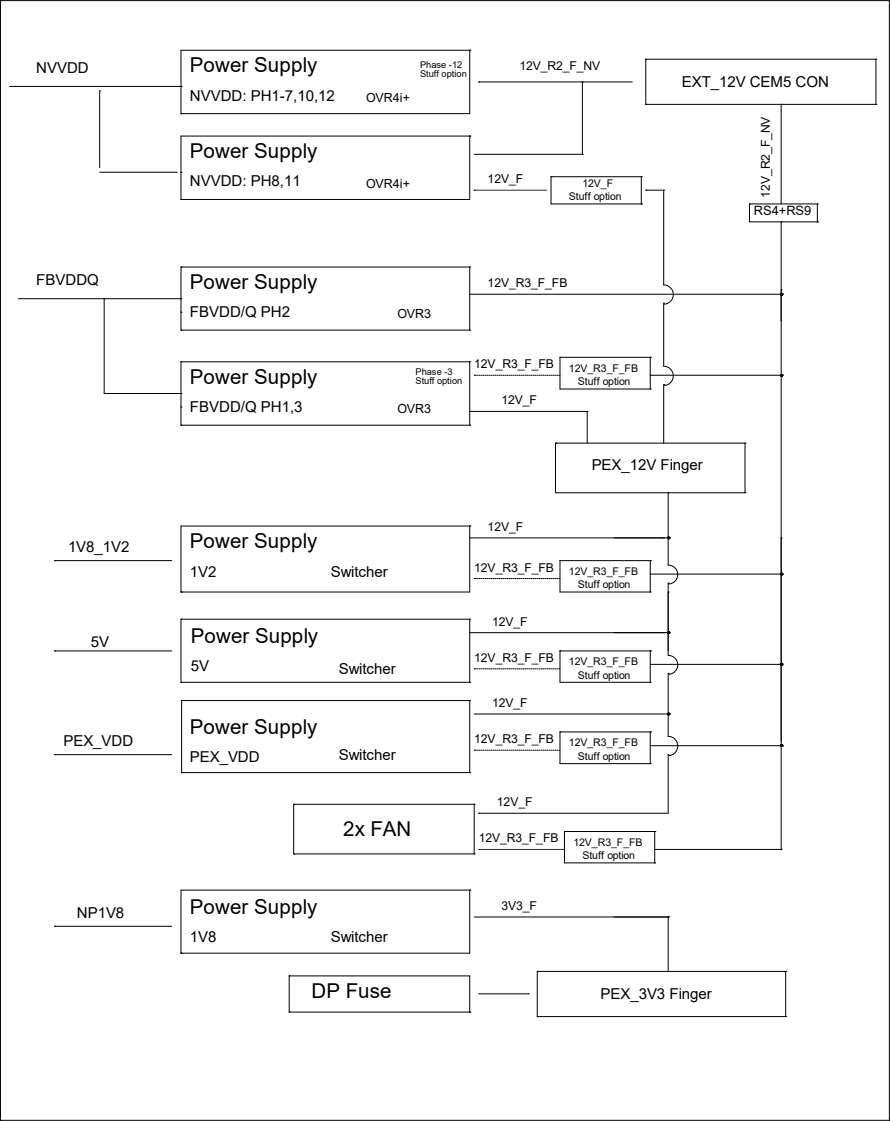
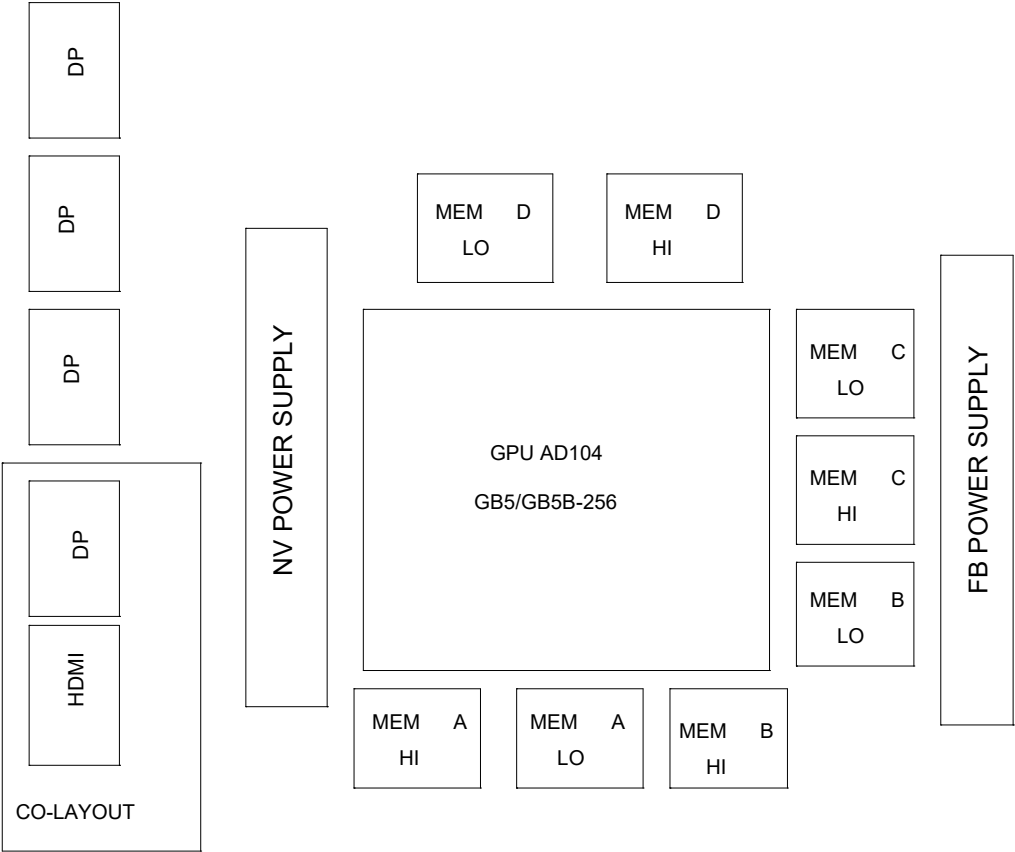
PG141-H00

AD104/NP GB5/5B-256 DESIGN, 16GB GDDRx, 256b, X16  
DP + DP + DP + HDMI/DP

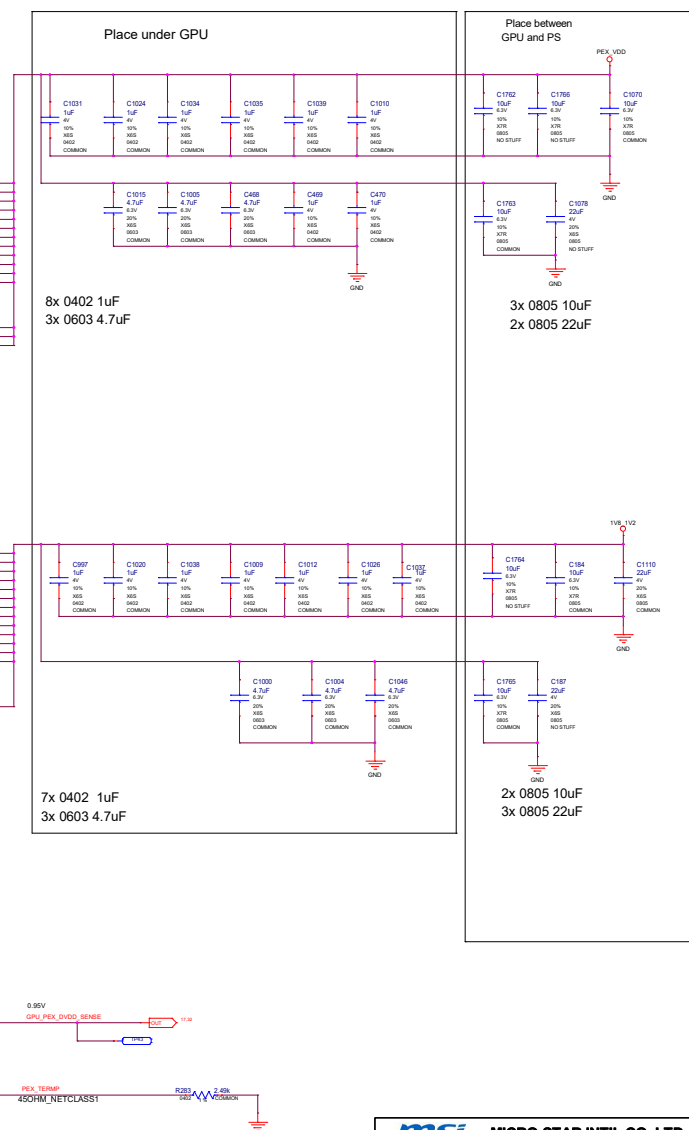
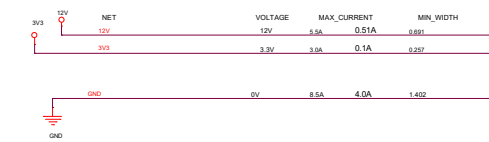
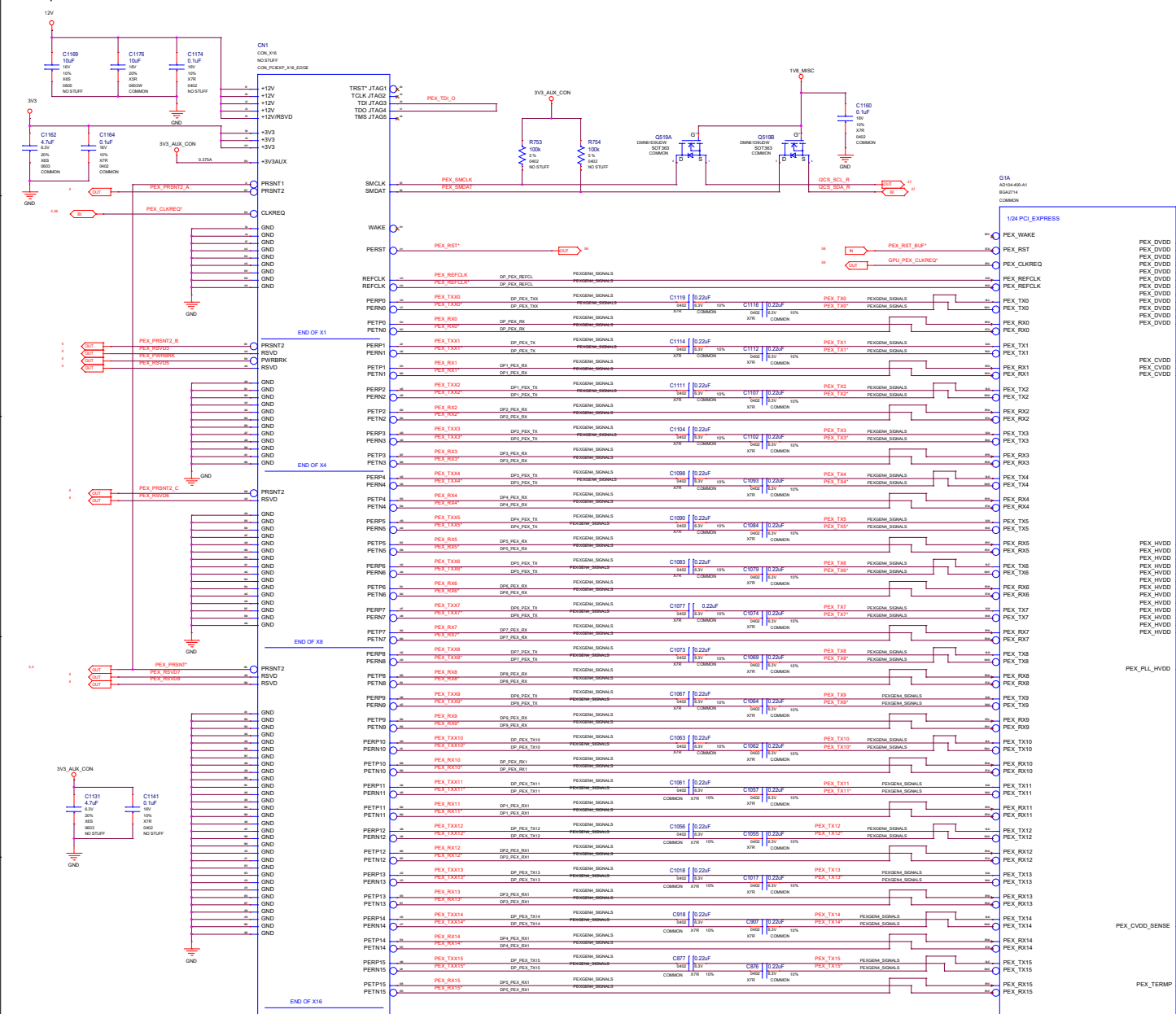
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Block Diagram



PCI Express

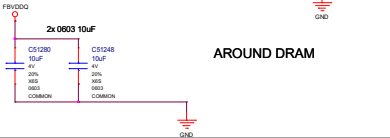
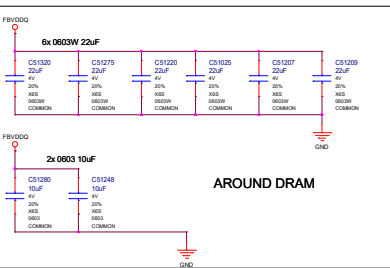
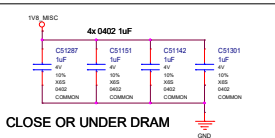
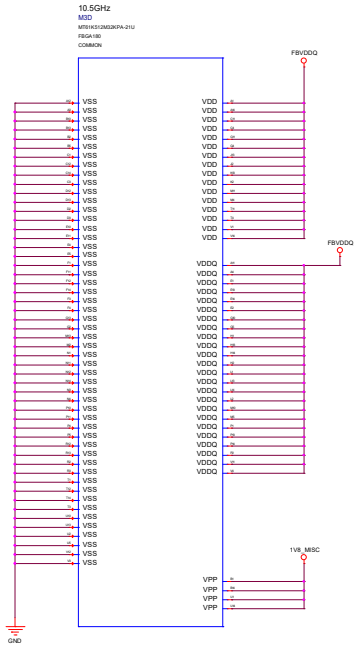


PCIE GEN4 RC TERMINATIONS





# MEMORY: FBA Partition 31..0

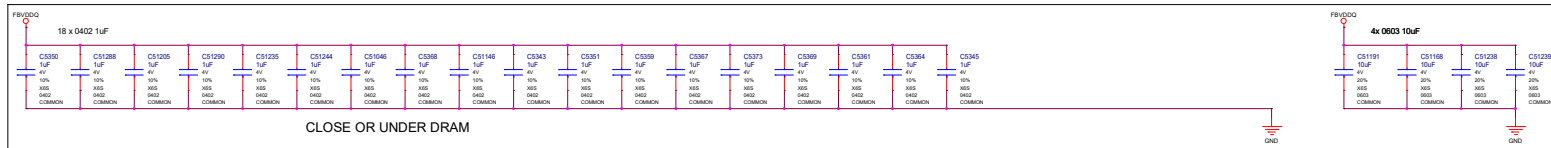


FBVDDQ DECAP per clamshell pair:

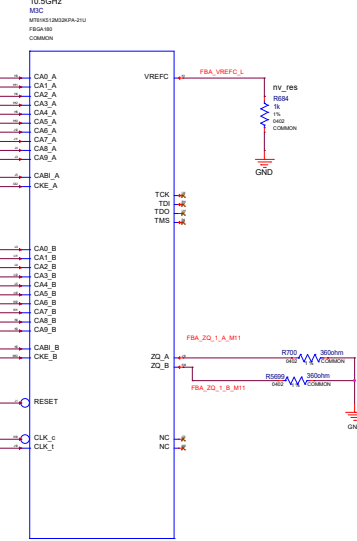
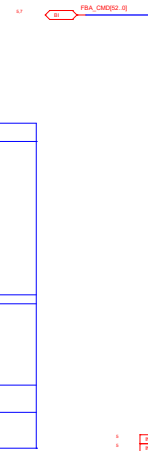
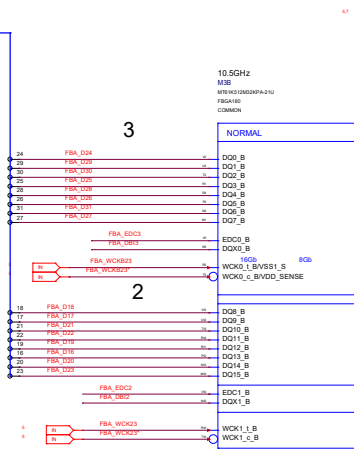
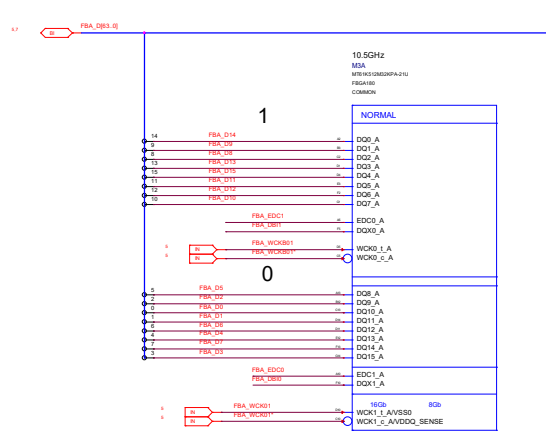
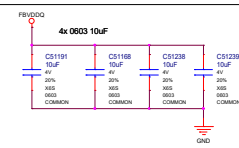
Close to DRAM:  
18x 1uF 0402  
4x 10uF 0603

Around DRAM:  
2x 10uF 0603  
6x 22uF 0603W

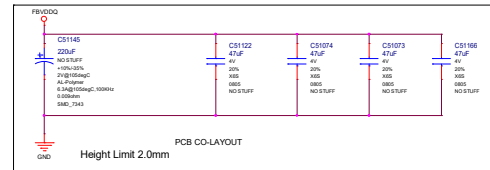
Need at least 2 gnd and 2 pwr vias per DECAP



CLOSE OR UNDER DRAM

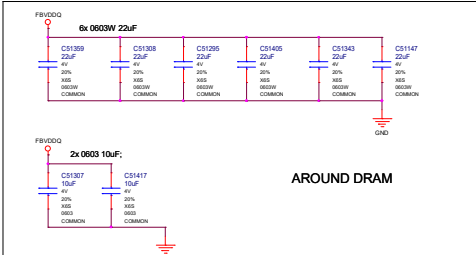
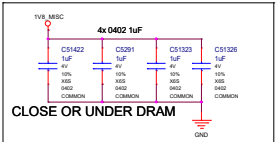
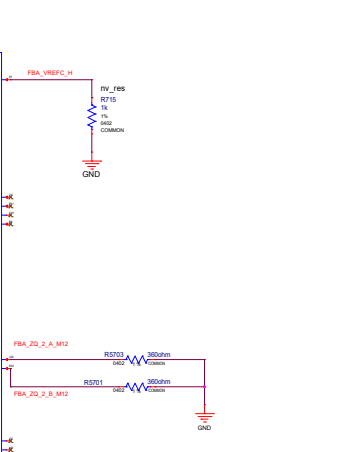
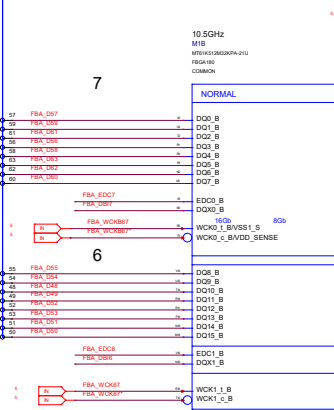
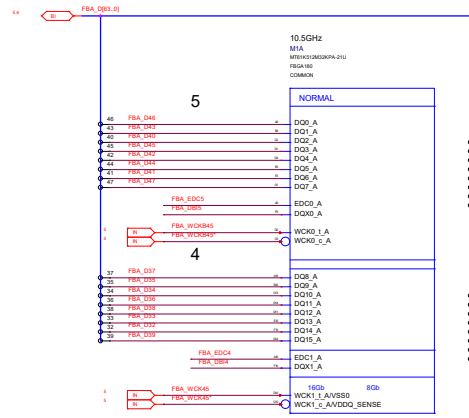
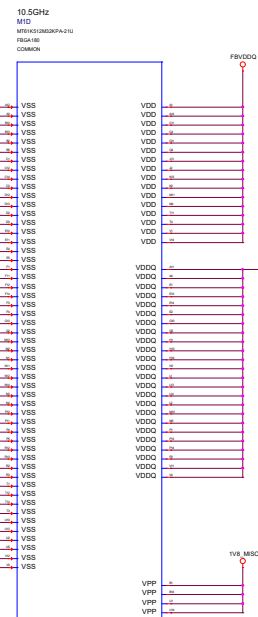


## UNDER DRAM



Height Limit 2.0mm

# MEMORY: FBA Partition 63..32

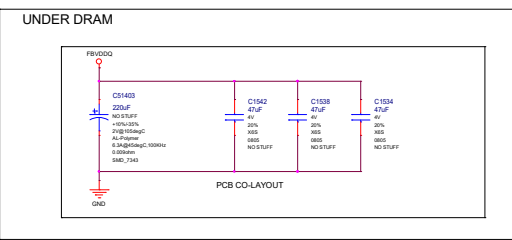
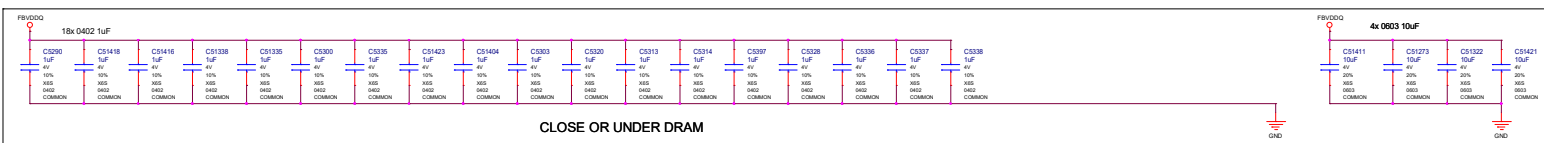


FBVDDQ DECAP per clamshell pair:

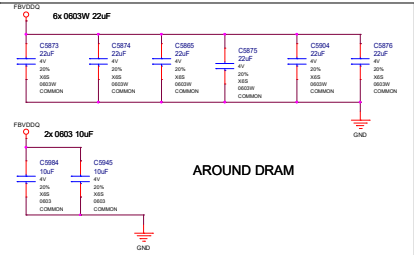
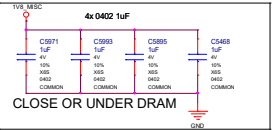
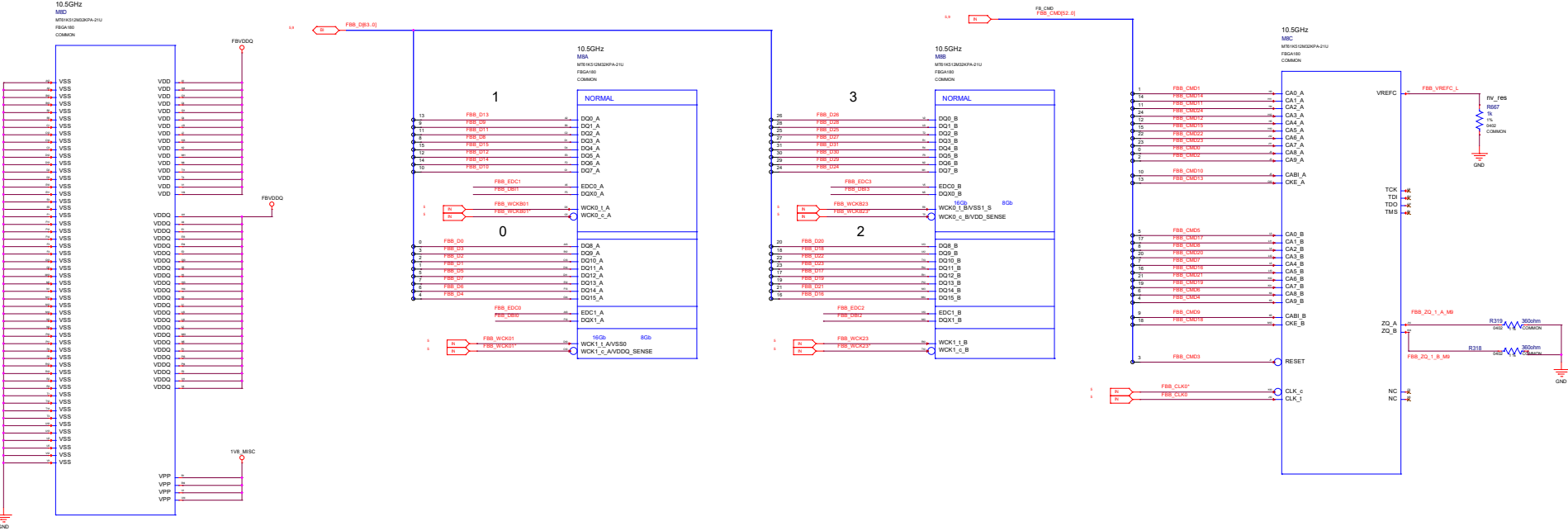
Close to DRAM: 18x 1uF 0402 4x 10uF 0603

Around DRAM: 2x 10uF 0603 6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP



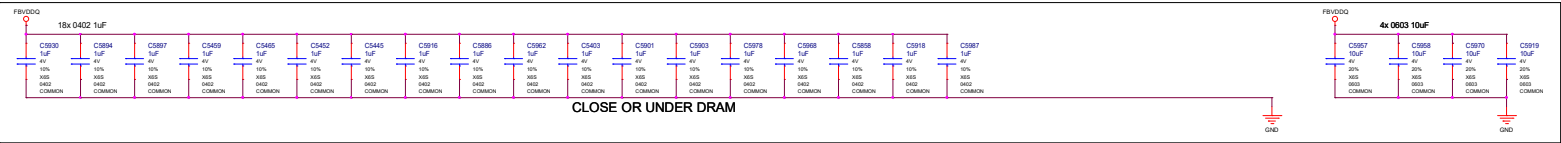
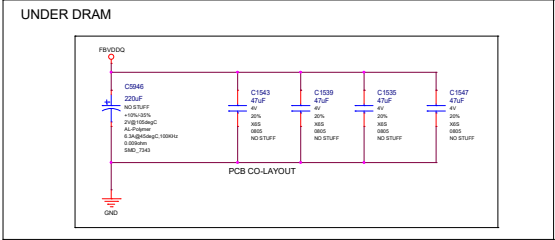
MEMORY: FBB Partition 31..0



FBVDDQ DECAP per clamshell pair:

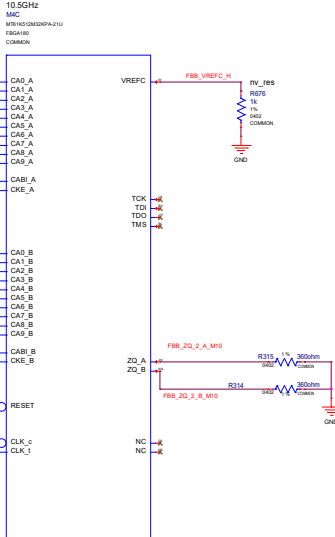
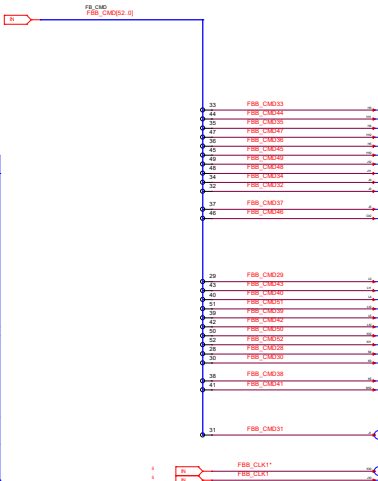
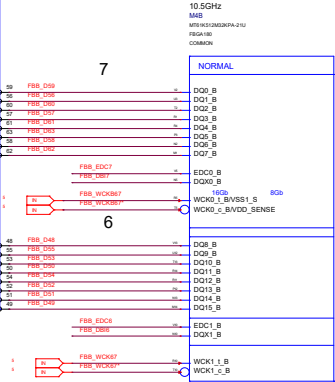
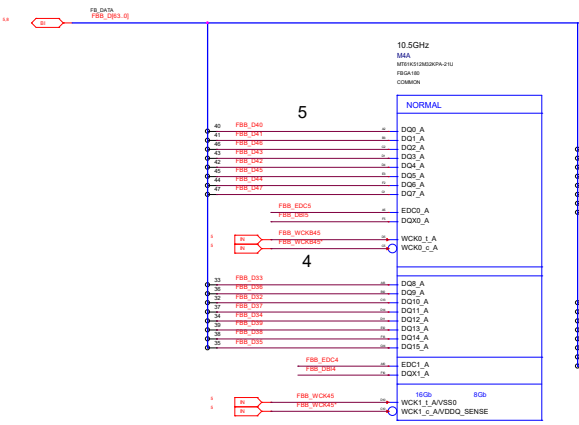
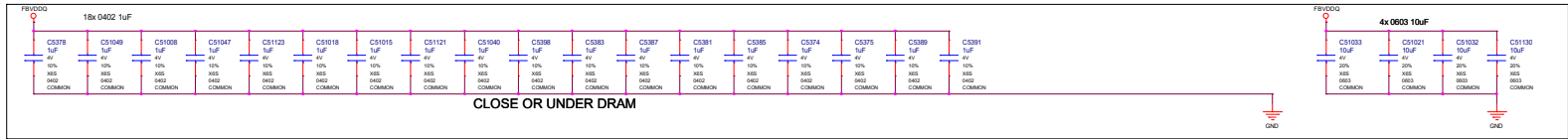
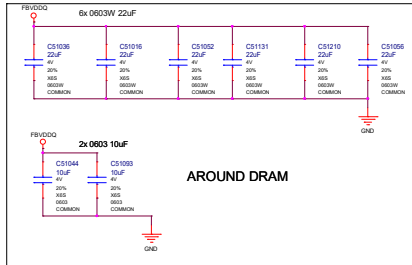
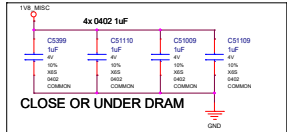
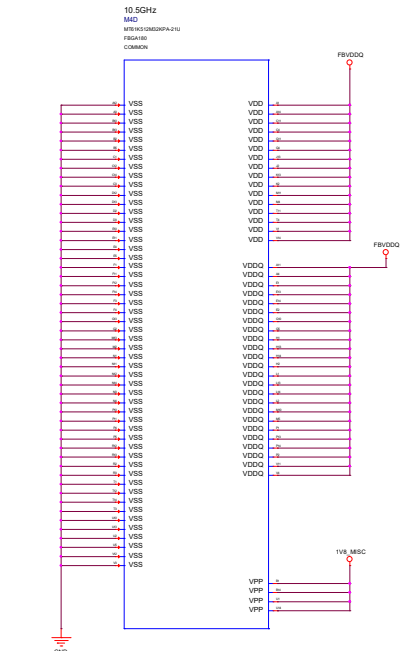
Close to DRAM:	Around DRAM:
18x 1uF 0402	2x 10uF 0603
4x 10uF 0603	6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP

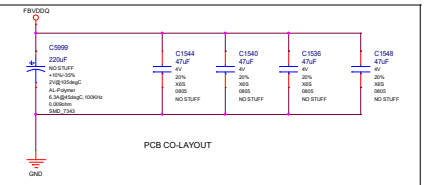




MEMORY: FBB Partition 63..32



UNDER DRAM

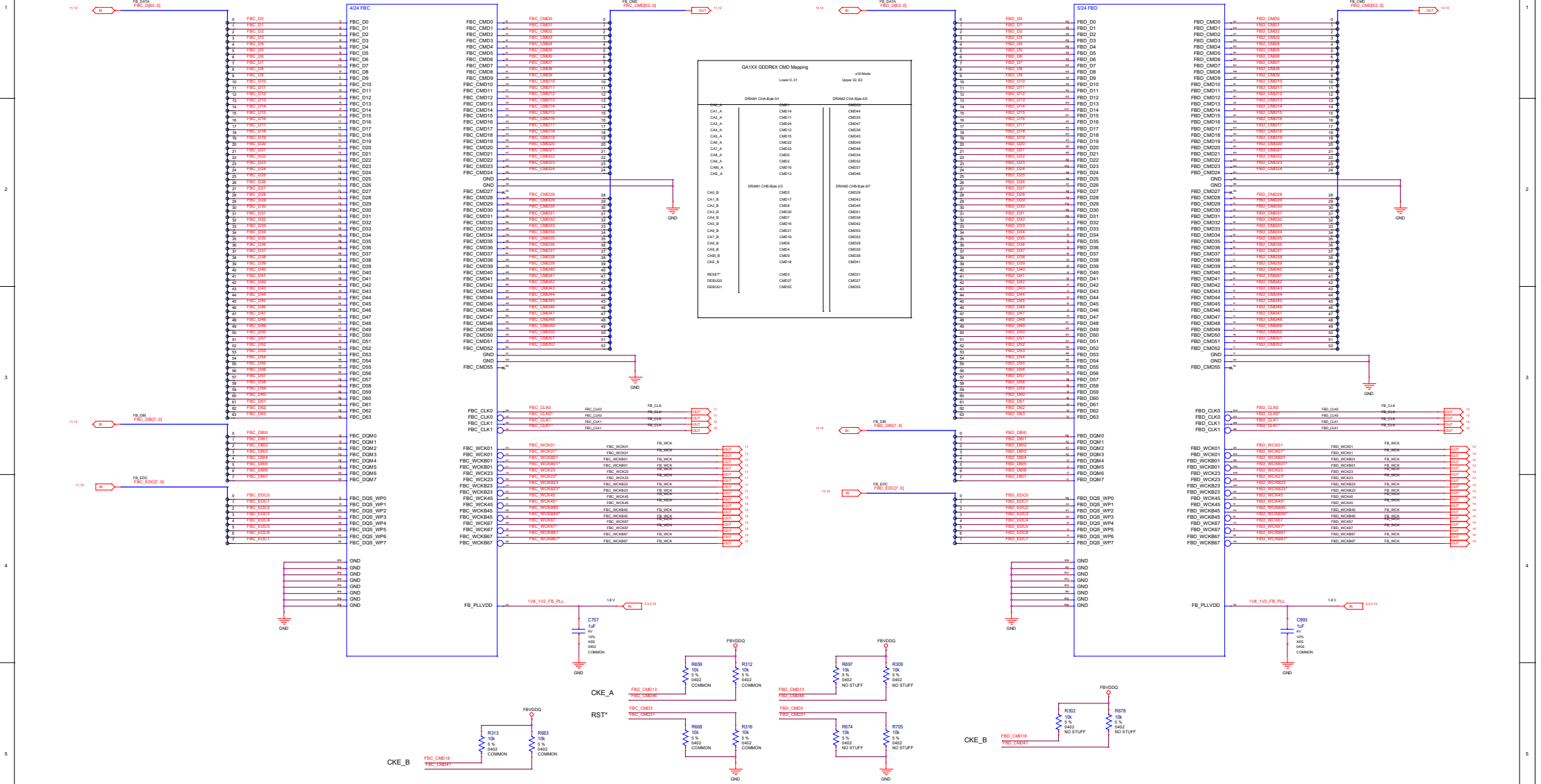


FBVDDQ DECAP per clamshell pair:

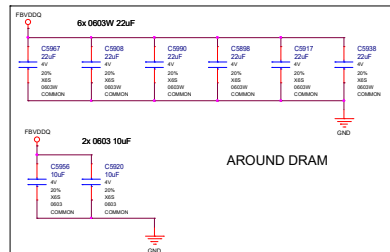
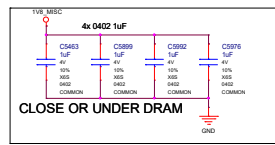
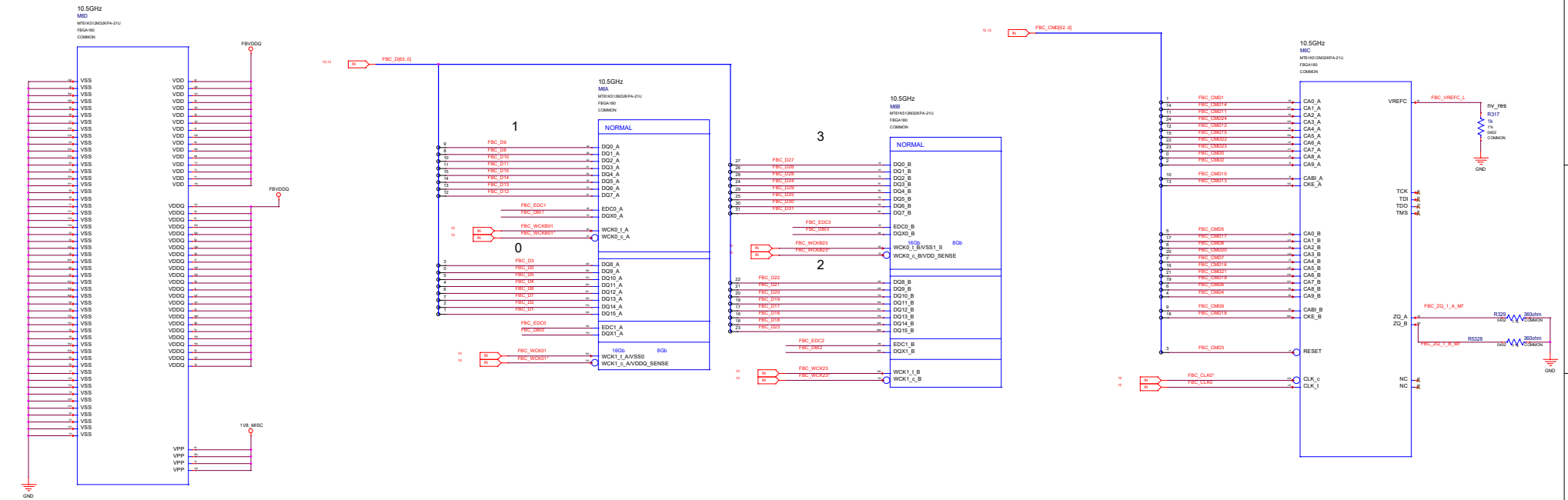
Close to DRAM:  
18x 1uF 0402  
4x 10uF 0603

Around DRAM:  
2x 10uF 0603  
6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP



MEMORY: FBC Partition 31..0



FBVDDQ DECAP per clamshell pair:

Close to DRAM:

18x 1uF 0402

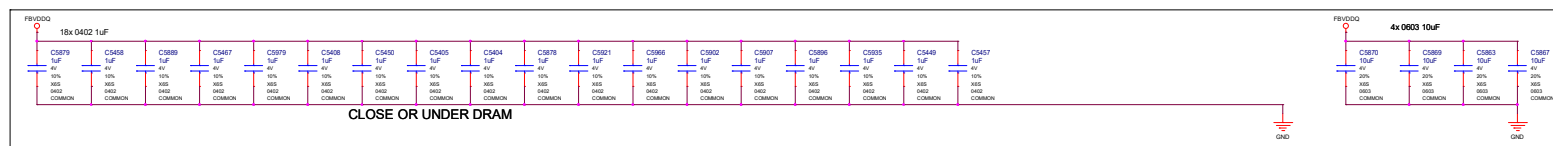
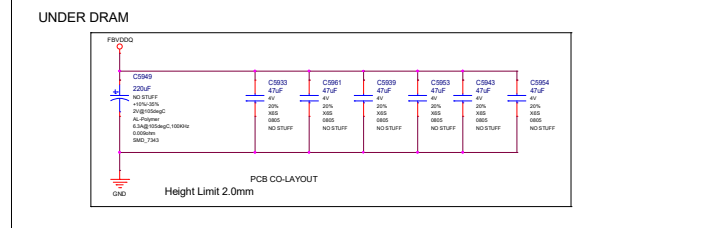
4x 10uF 0603

Around DRAM:

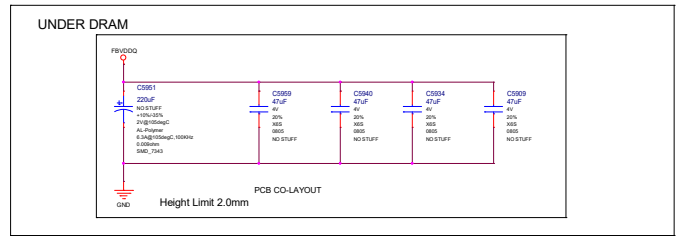
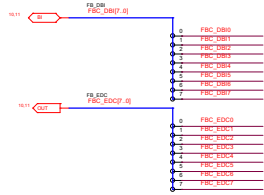
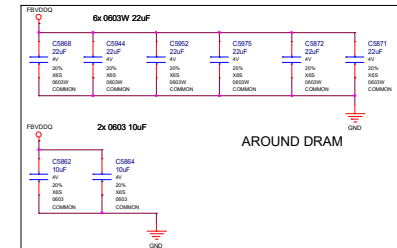
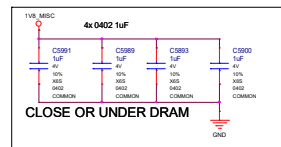
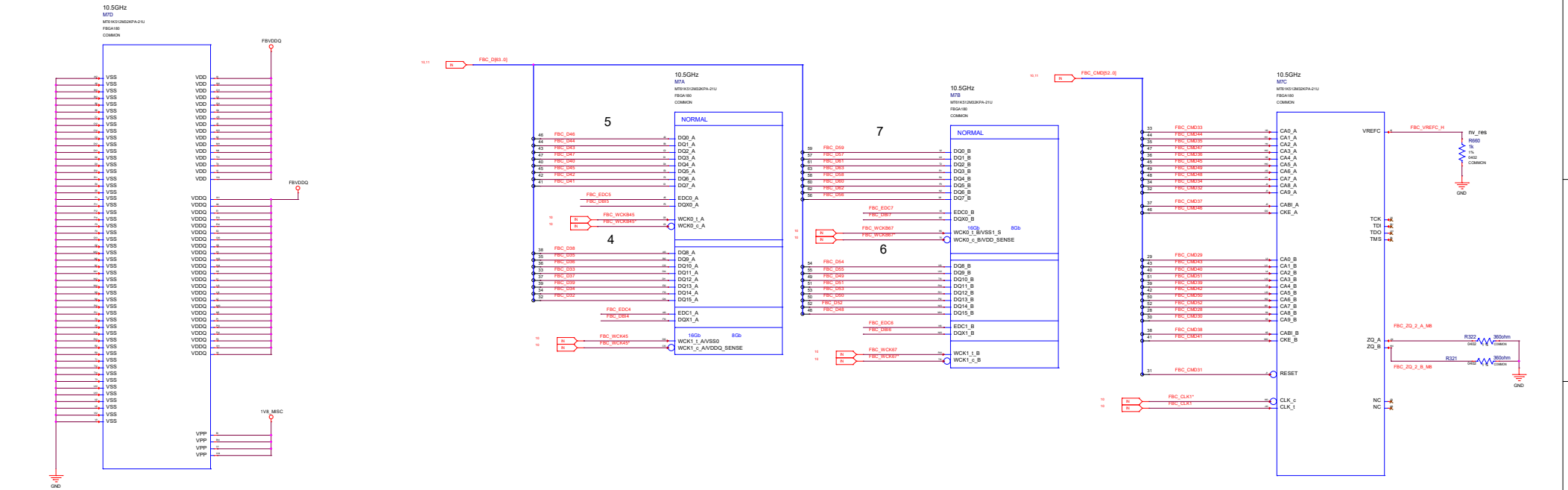
2x 10uF 0603

6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP



MEMORY: FBC Partition 63..32



FBVDDQ DECAP per clamshell pair:

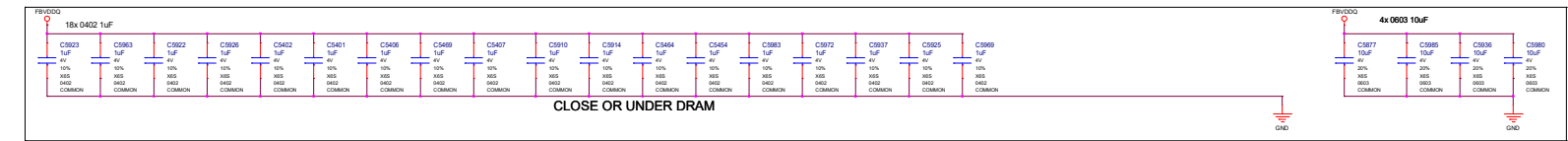
Close to DRAM:

10x	1uF	0402
4x	10uF	0603

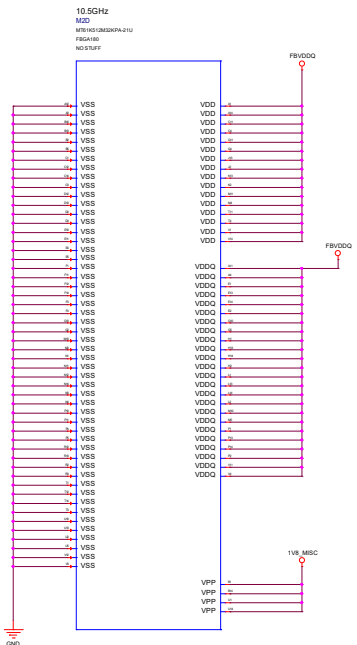
Around DRAM:

2x 10uF 0603

Need at least 2 gnd and 2 pwr vias per DECAP



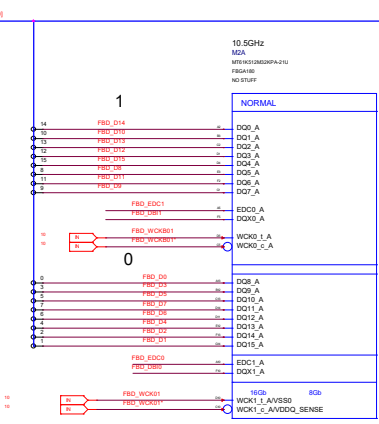
# MEMORY: FBD Partition 31..0



10.14 FB\_D03\_0

10.14 FB\_D03\_0

1V8 M5C



10.14 FB\_D03\_0

10.14 FB\_D03\_0

1V8 M5C



10.14 FB\_D03\_0

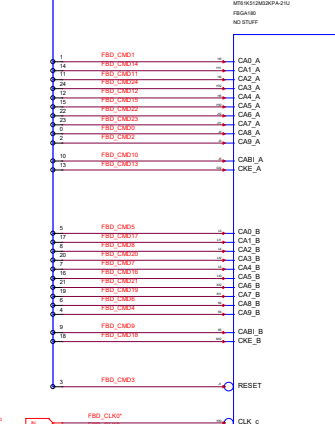
10.14 FB\_D03\_0

1V8 M5C

10.14 FB\_D03\_0

10.14 FB\_D03\_0

1V8 M5C



10.14 FB\_D03\_0

10.14 FB\_D03\_0

1V8 M5C

10.14 FB\_D03\_0

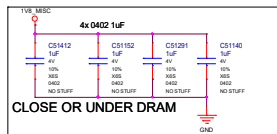
10.14 FB\_D03\_0

1V8 M5C

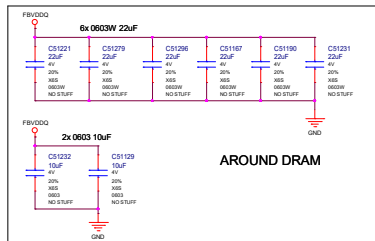
10.14 FB\_D03\_0

10.14 FB\_D03\_0

1V8 M5C



CLOSE OR UNDER DRAM



AROUND DRAM

FBVDDQ DECAP per clamshell pair:

Close to DRAM:

18x 1uF 0402

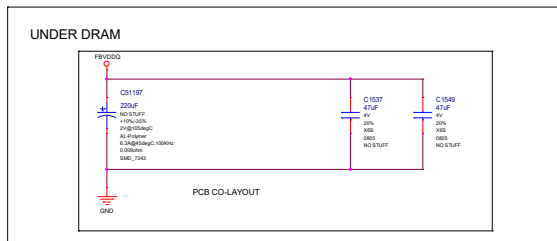
4x 10uF 0603

Around DRAM:

2x 10uF 0603

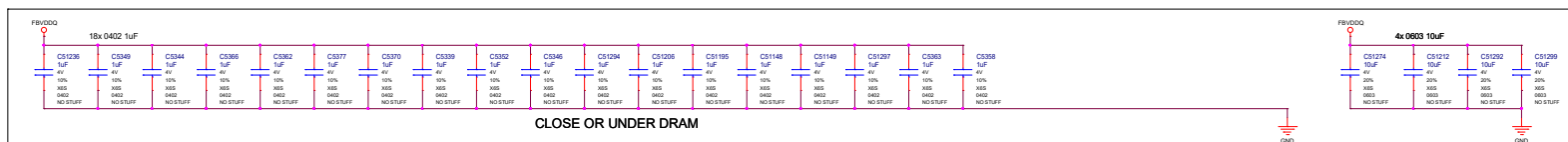
6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP



UNDER DRAM

PCB CO-LAYOUT



CLOSE OR UNDER DRAM

10.14 FB\_D03\_0

10.14 FB\_D03\_0

MEMORY: FBD Partition 63..32

10.5GHz  
M52  
M52V3300000PA21U  
FPGA180  
NO STUFF



10.13

FBD\_QB3\_0

10.13

FBD\_QB3\_0

10.13

FBD\_QB3\_0

10.13

FBD\_QB3\_0

10.13

FBD\_QB3\_0

10.13

FBD\_QB3\_0

10.13

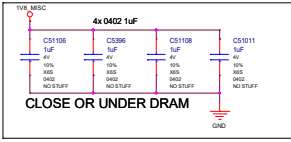
FBD\_QB3\_0

10.13

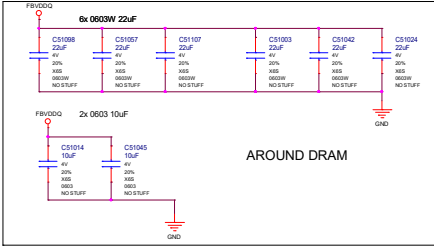
FBD\_QB3\_0

10.13

FBD\_QB3\_0



CLOSE OR UNDER DRAM



AROUND DRAM

FBVDDQ DECAP per clamshell pair:

Close to DRAM:

18x 1uF 0402

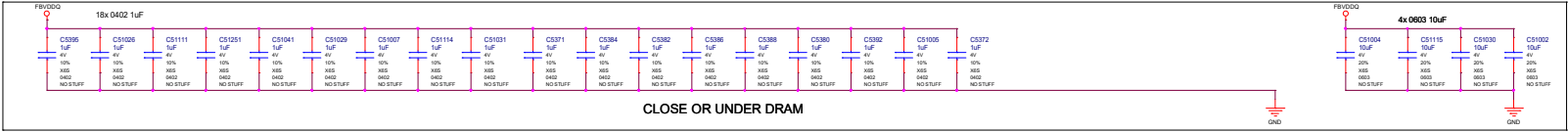
4x 10uF 0603

Around DRAM:

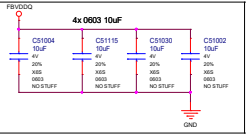
2x 10uF 0603

6x 22uF 0603W

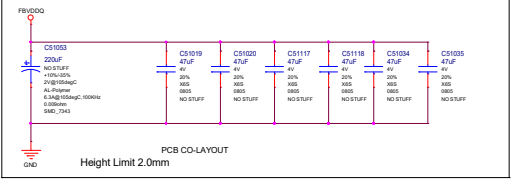
Need at least 2 gnd and 2 pwr vias per DECAP



CLOSE OR UNDER DRAM



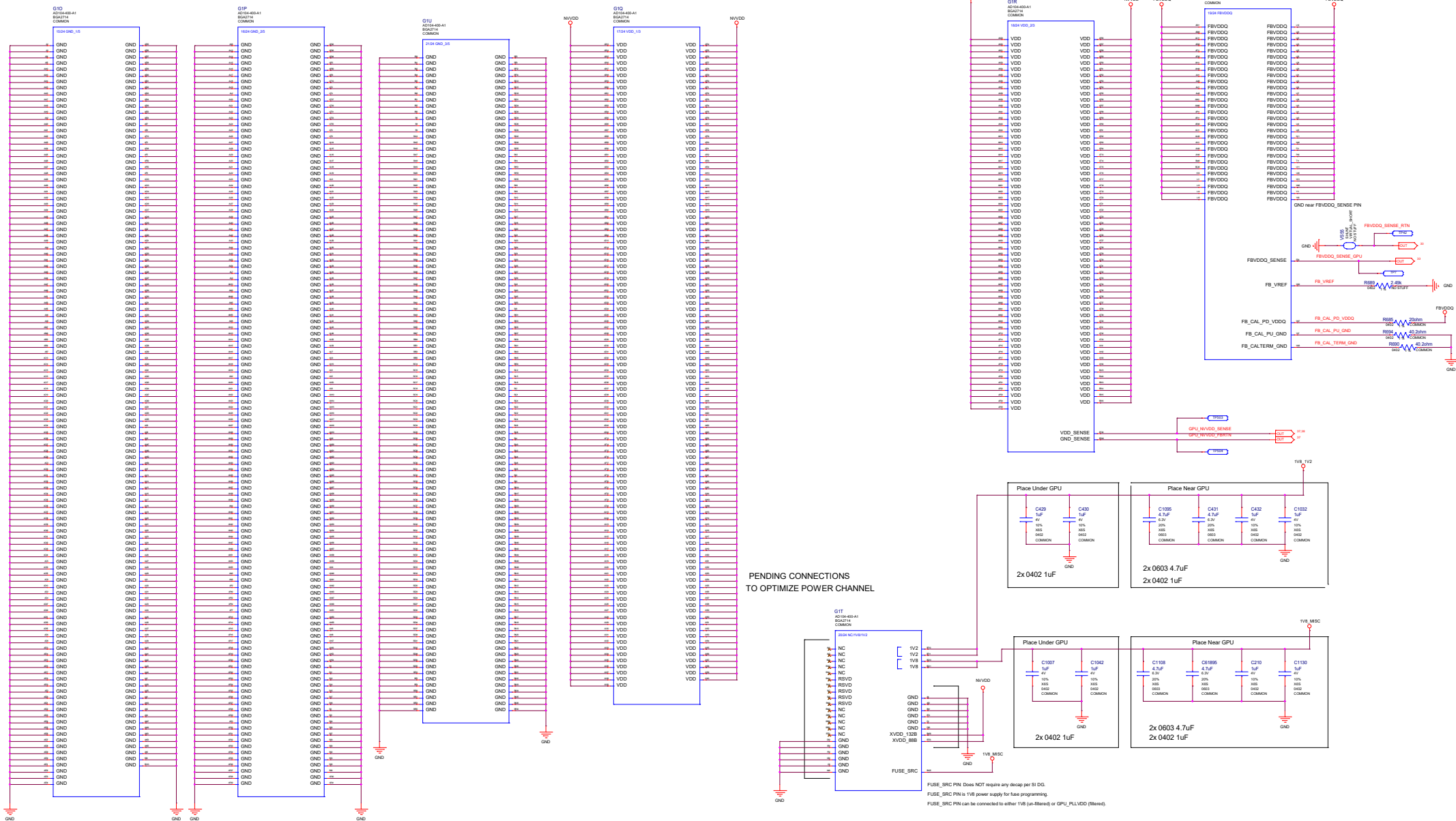
UNDER DRAM



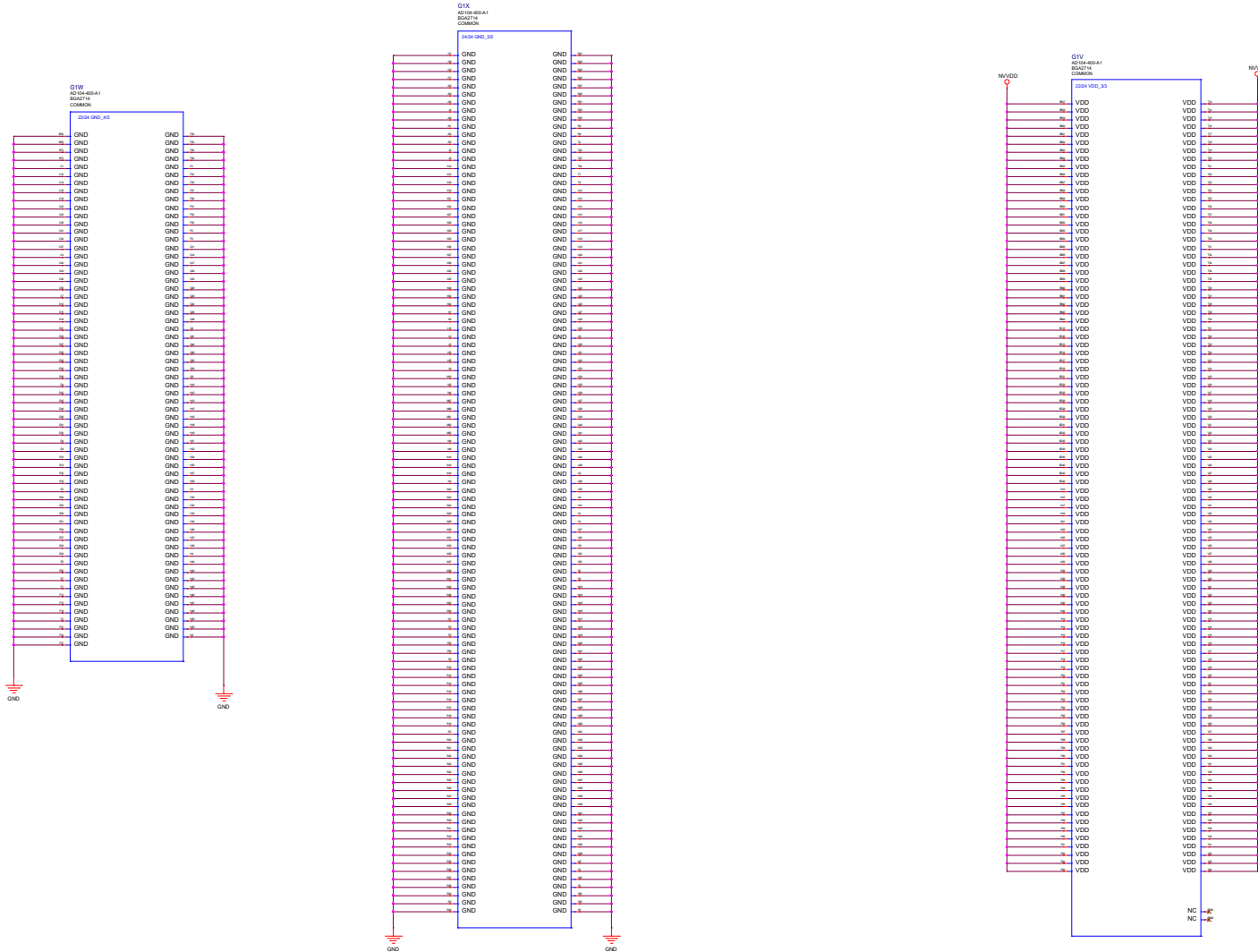
PCB CO-LAYOUT

Height Limit 2.0mm

## GPU PWR and GND

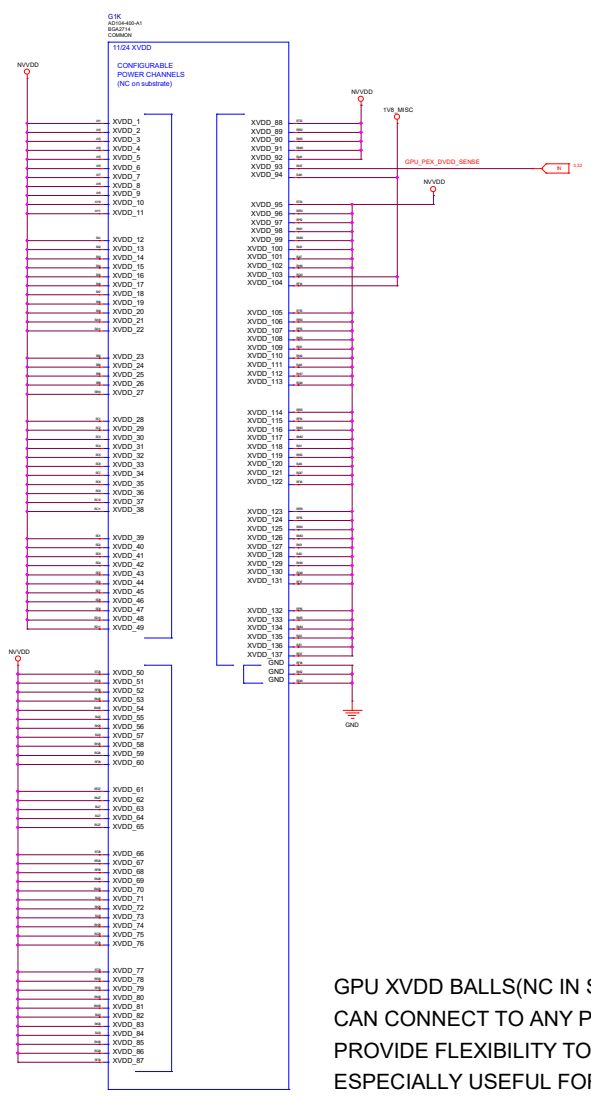


GPU PWR and GND 2





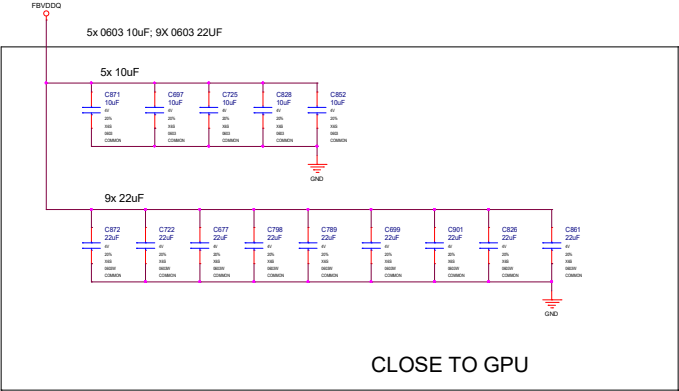
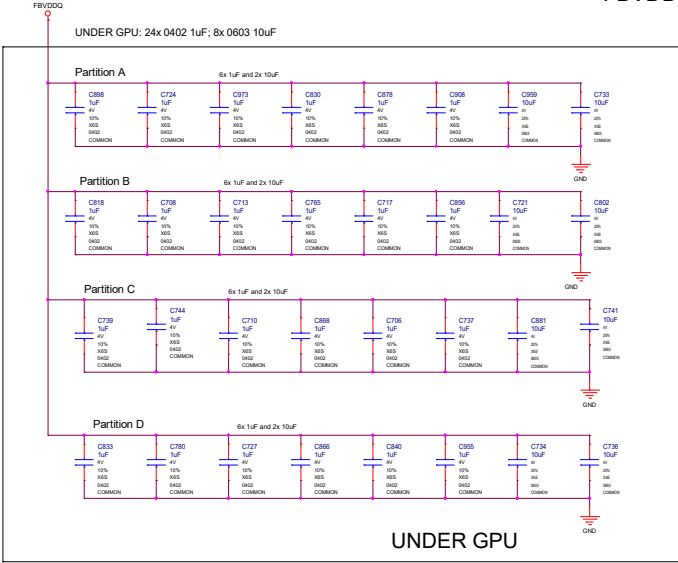
XVDD



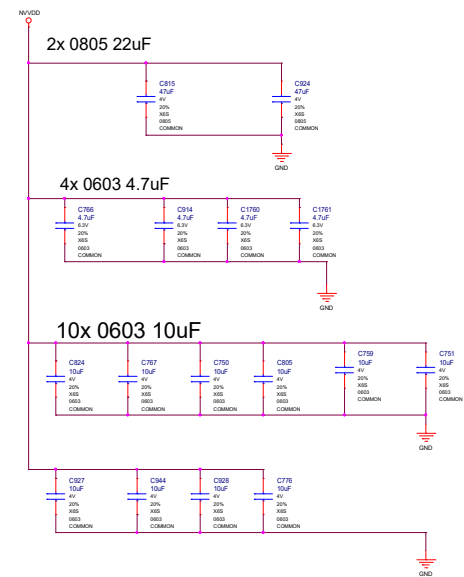
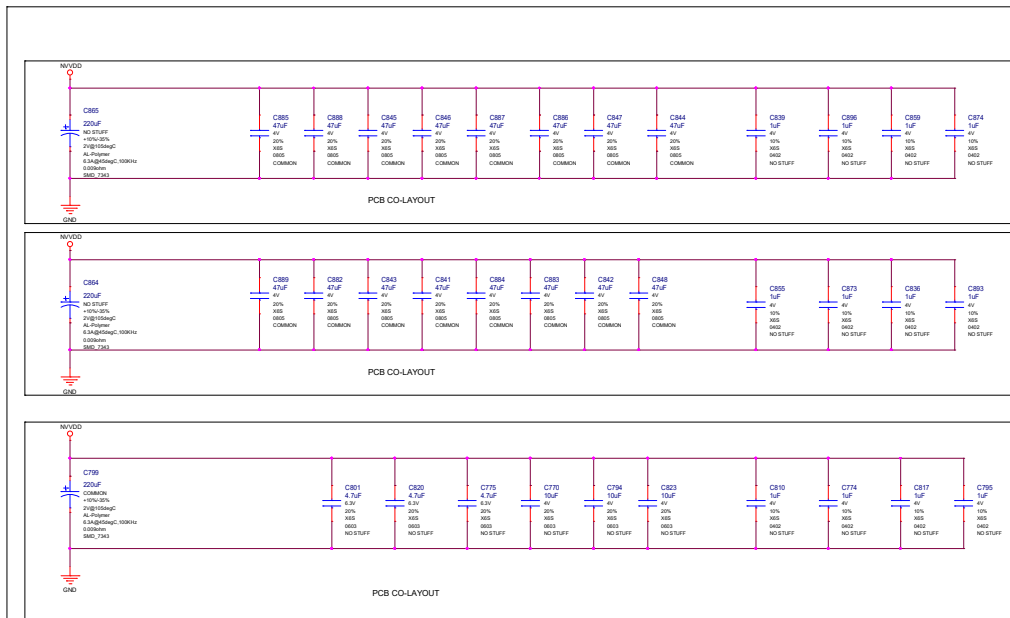
GPU XVDD BALLS(NC IN SUBSTRATE):  
CAN CONNECT TO ANY POWER NET(NV/MS/1V8/PEX,etc) ON SYSTEM BOARD,  
PROVIDE FLEXIBILITY TO OPTIMIZE POWER CHANNELS ON SYSTEM BOARD,  
ESPECIALLY USEFUL FOR LOW-COST DESIGN WITH REDUCED PCB LAYERS.

GPU DECOUPLING FBVDDQ

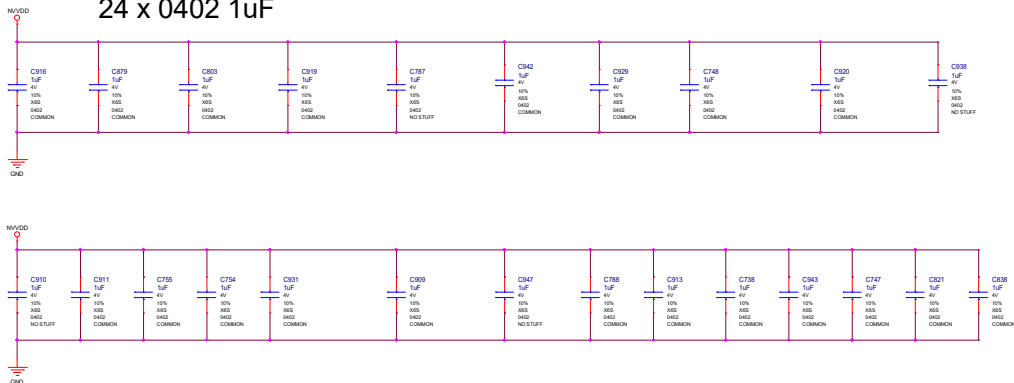
FBVDDQ



## GPU DECOUPLING NVDD

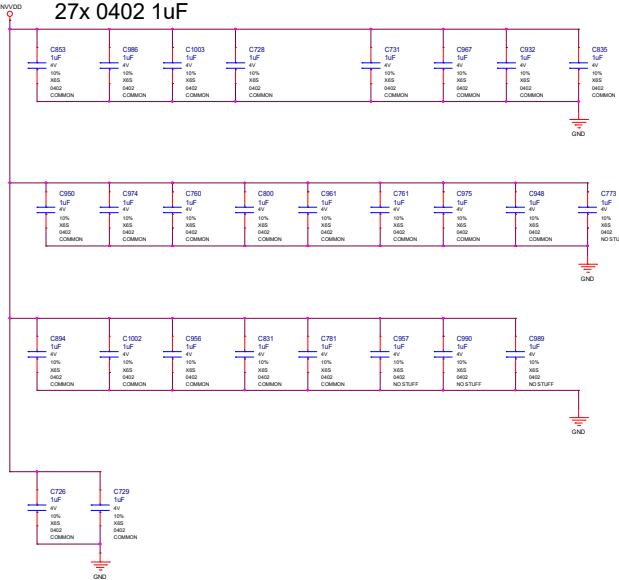
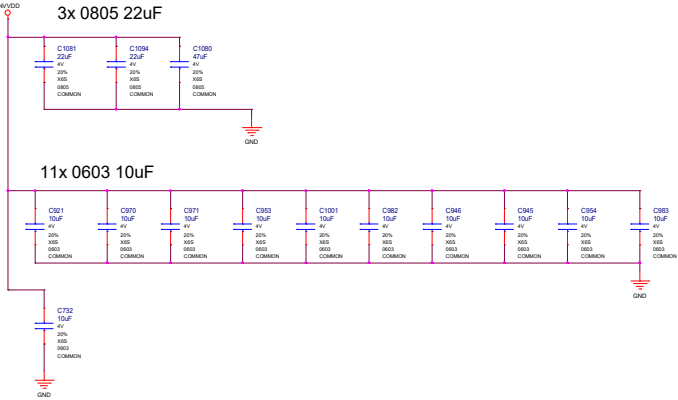
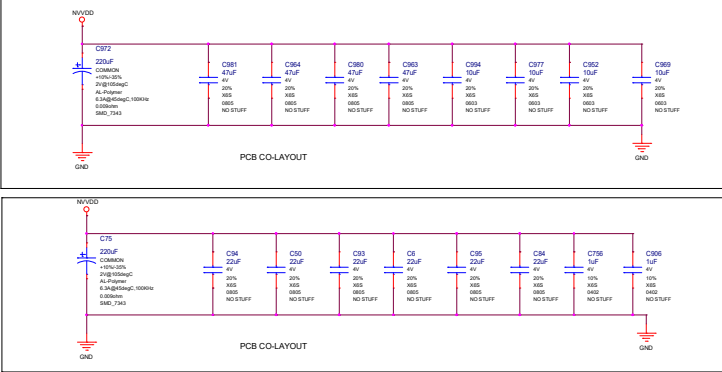


24 x 0402 1uF



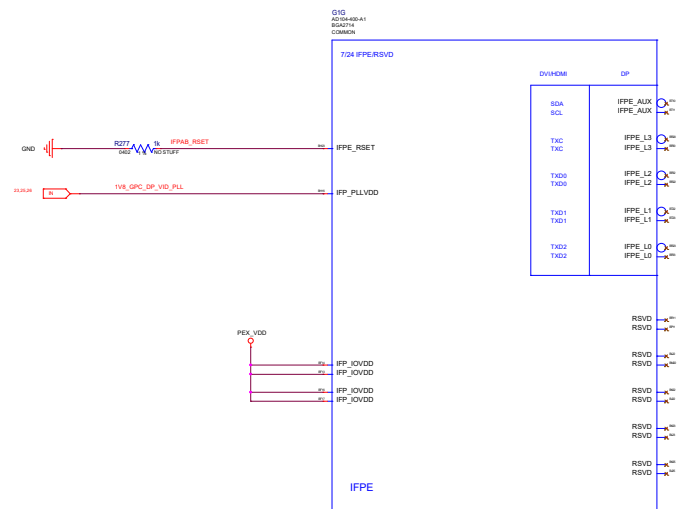
UNDER GPU

GPU DECOUPLING NVVDD



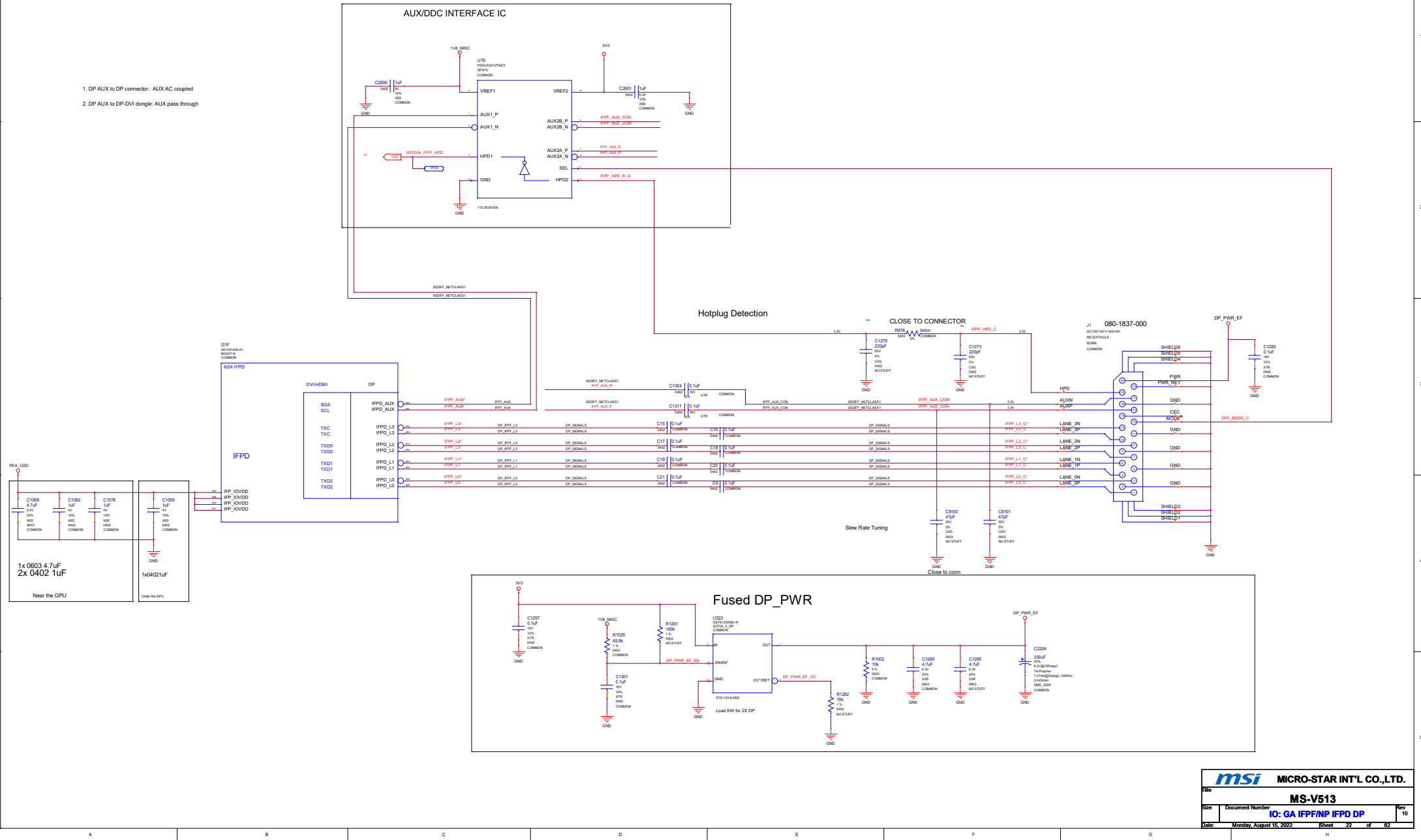
UNDER GPU

## GA IFPA/NP IFPE(NC)



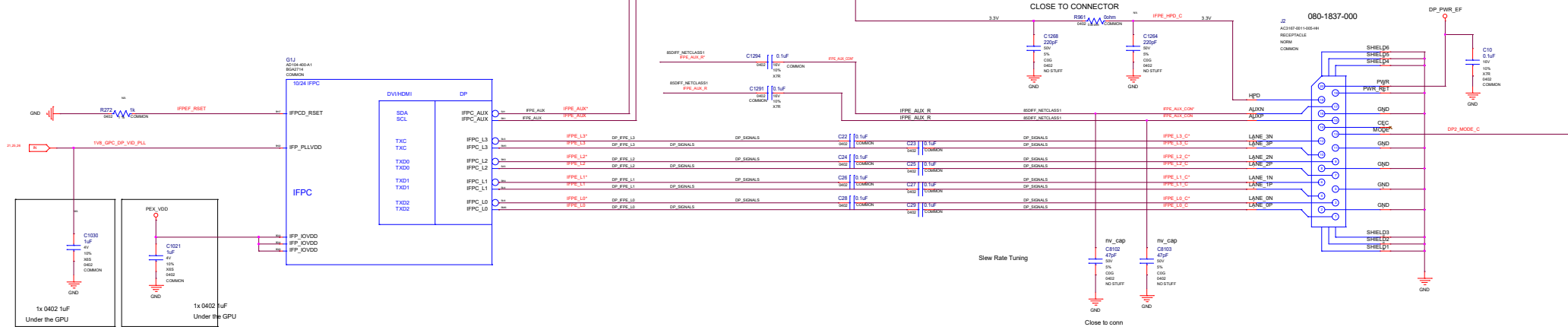
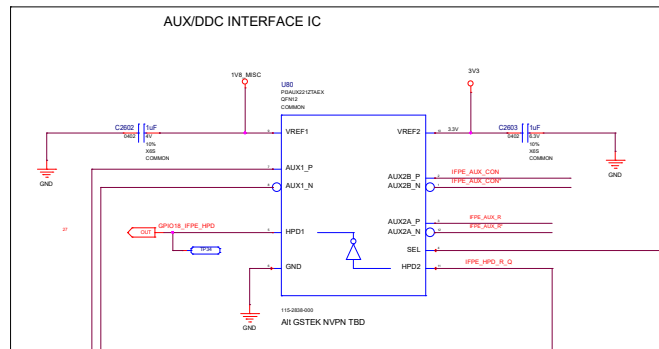
# GA IFPF/NP IFPD DP

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



## GA IFPE/NP IFPC DP

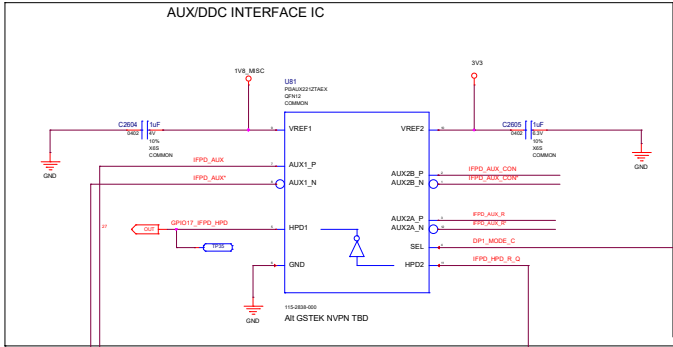
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



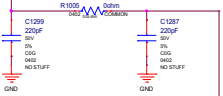
GA IFPD/NP IFPB DP

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

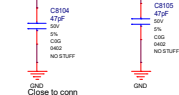
AUX/DDC INTERFACE IC



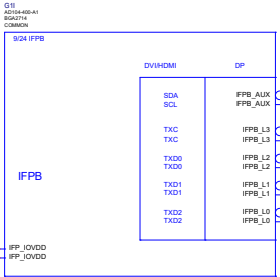
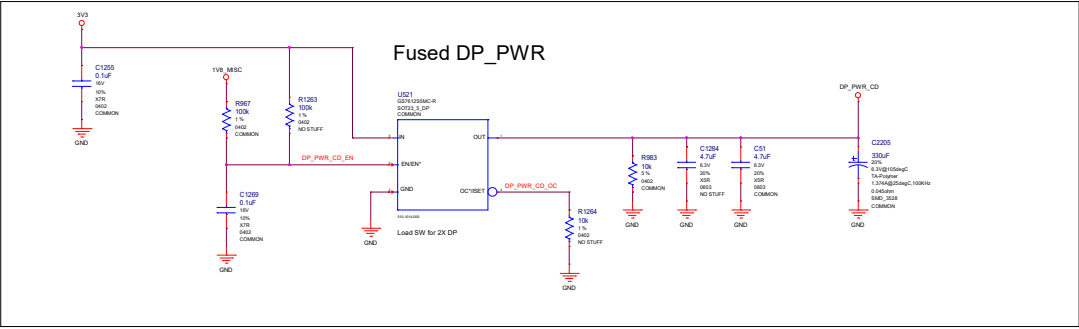
Hotplug Detection



Slew Rate Tuning



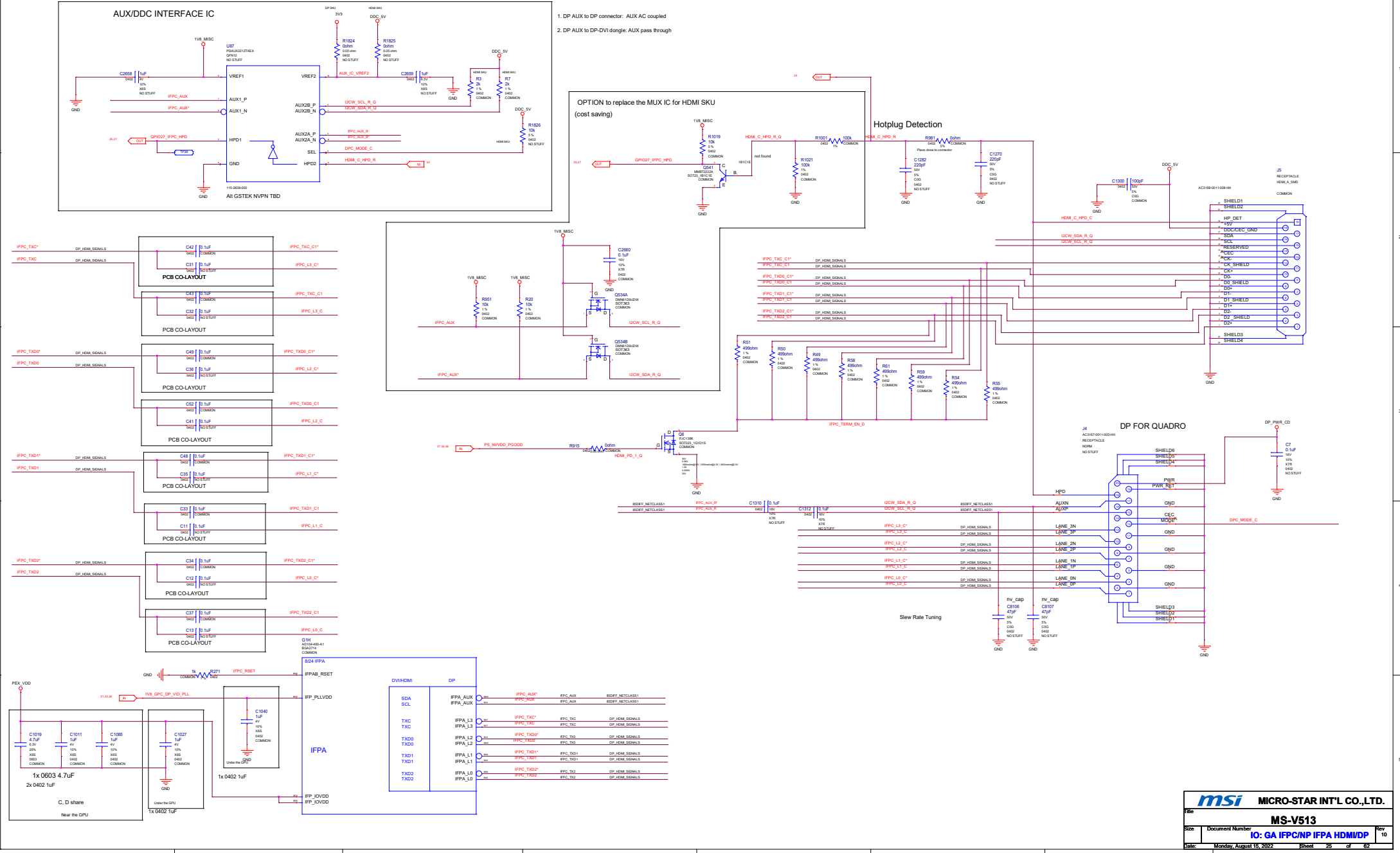
Fused DP\_PWR



1x 0402 1uF  
(was 1x 0201W 0.47uF)

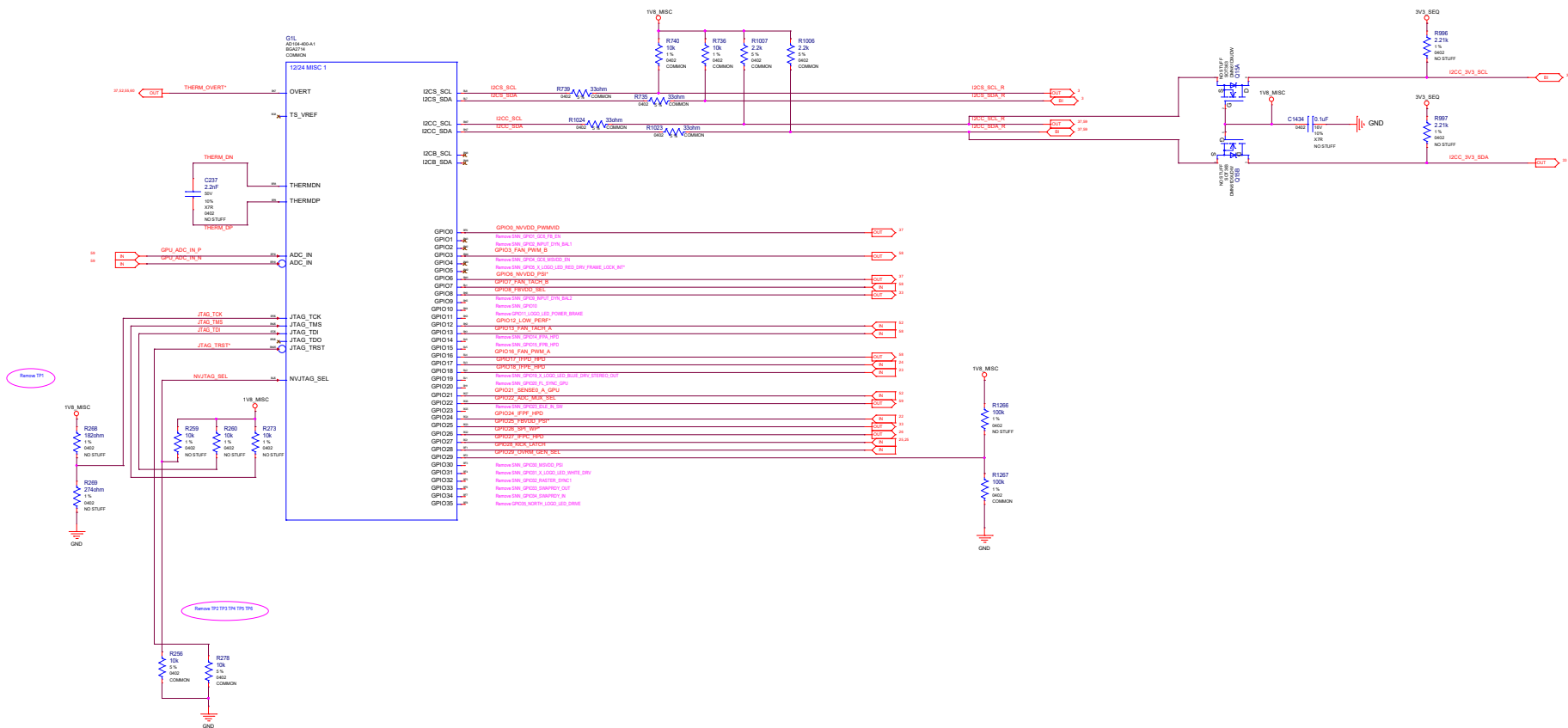


GA IFPC/NP IFPA HDMI/DP co-layout





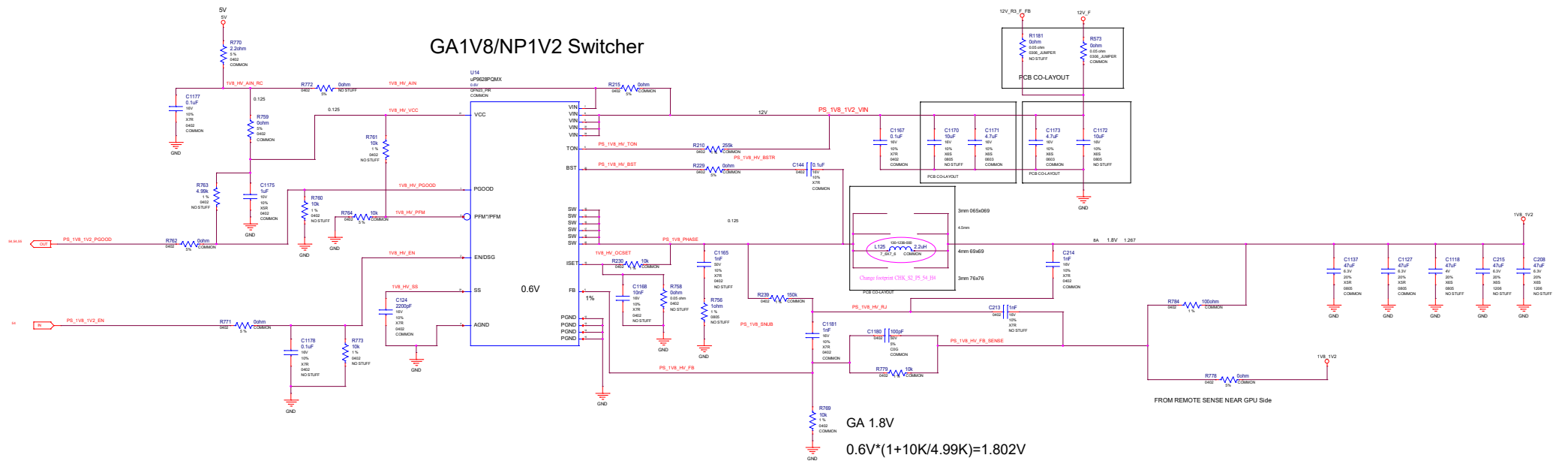
## MISC1: JTAG, GPIO, ADC, I2C, OVERT



XV RGB LED

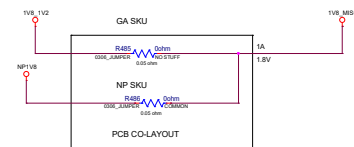
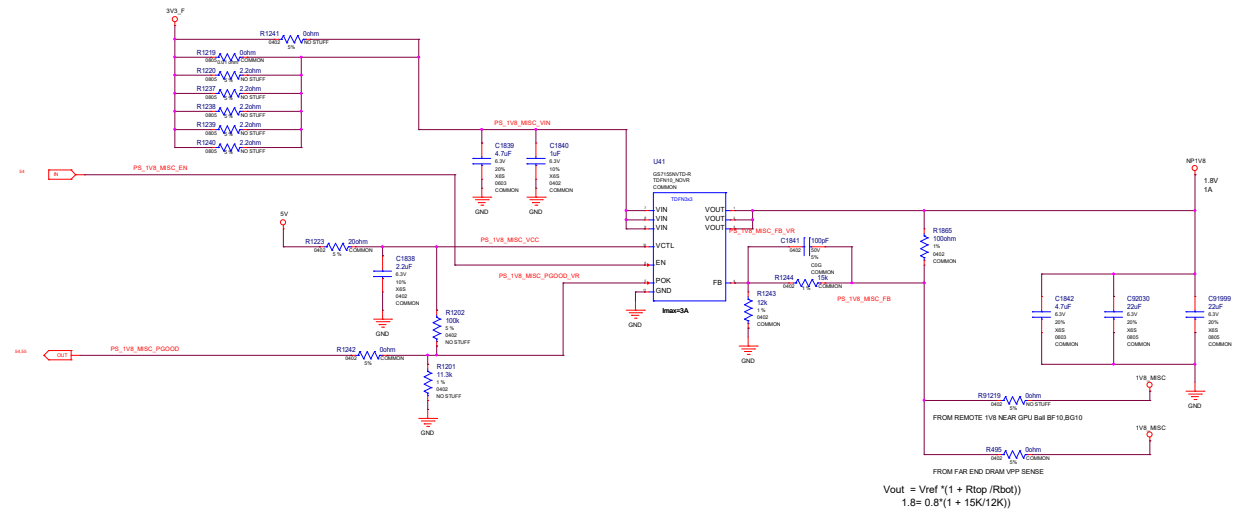
DELETED ID LED CKT; NOT SUPPORTED ON MEITNER

## GA1V8/NP1V2 Switcher




GA 1.8V  
 $0.6V \cdot (1 + 10K/4.99K) = 1.802V$   
 NP 1.2V  
 $0.6V \cdot (1 + 10K/10K) = 1.2V$

## NP1V8





 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	<b>MS-V513</b>
Size	<b>PS: 5V</b>
Document Number	Rev 10
Date: Monday, August 15, 2022	Sheet 31 of 62

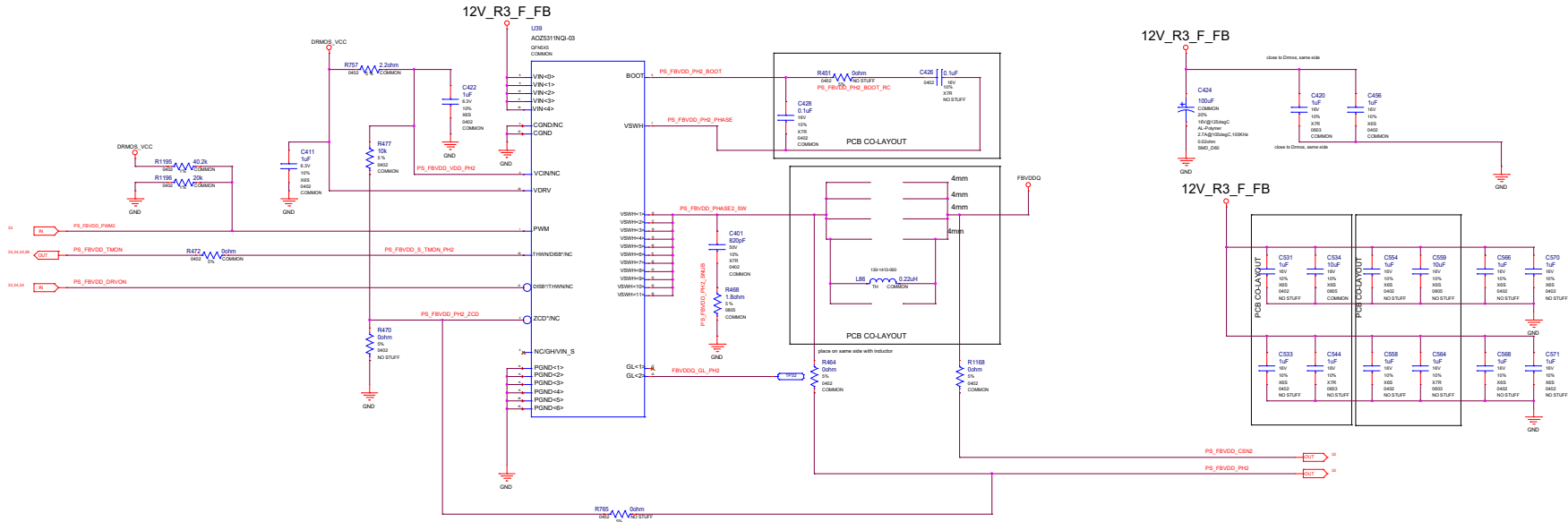




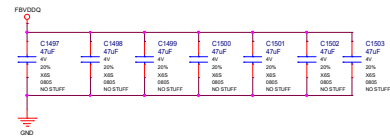
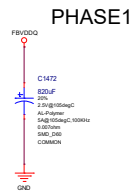




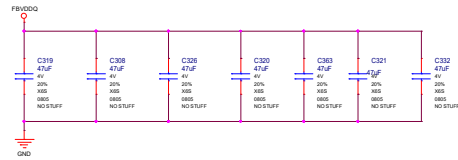
FBVDDQ PH2



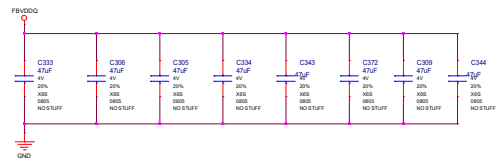
## FBVDDQ OUTPUT CAP



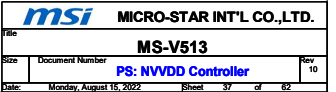
## PHASE2



### PHASE3



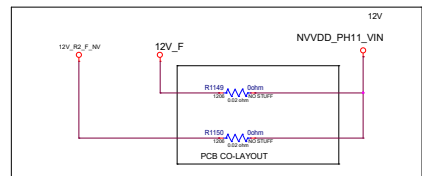
Support:  
MP2898,UP9512,RT8848,NCP81610 with DCR SENSE  
MP2888 With IMON SENSE



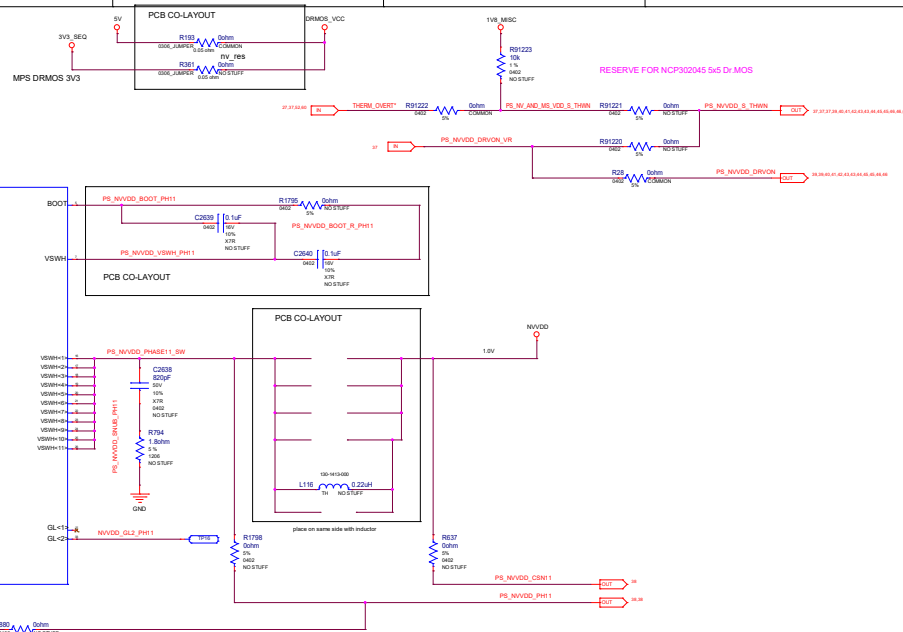
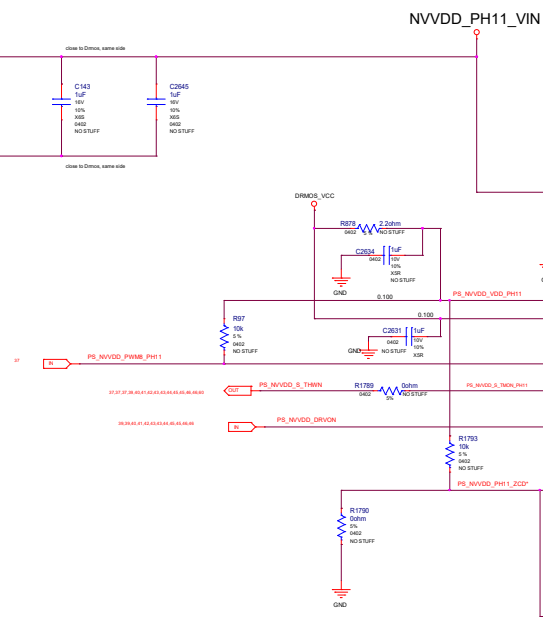
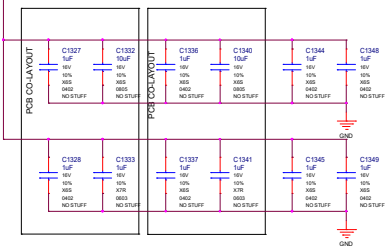


# NVVDD PH11 & PH8

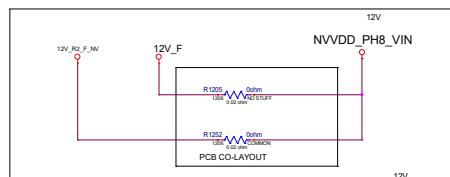
## NVVDD PH11(PWM8)



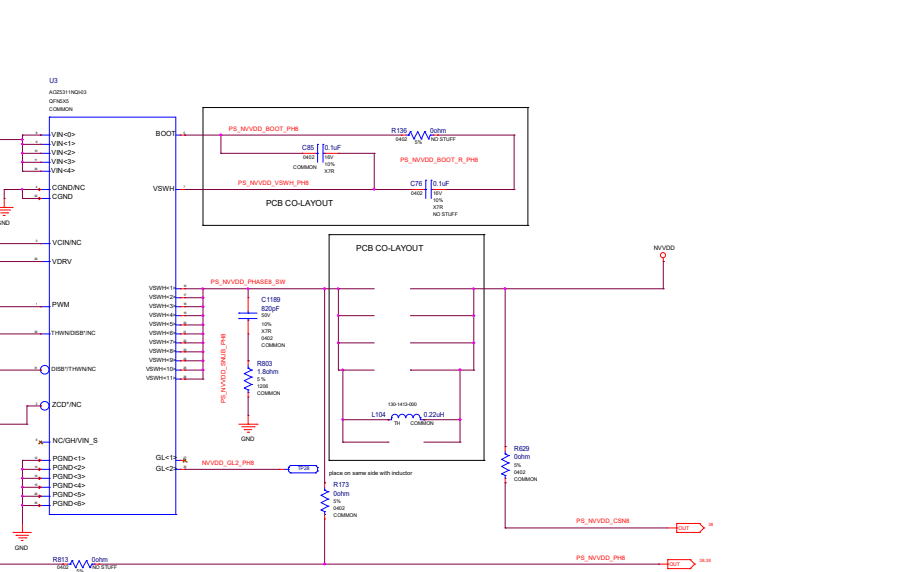
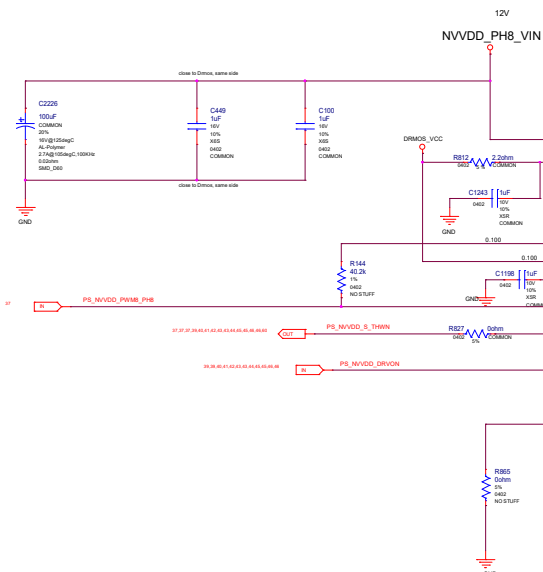
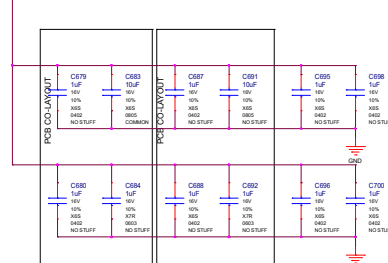
### NVVDD PH11\_VIN



## NVVDD PH8(PWM8)



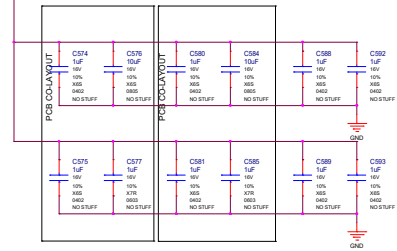
### NVVDD PH8\_VIN



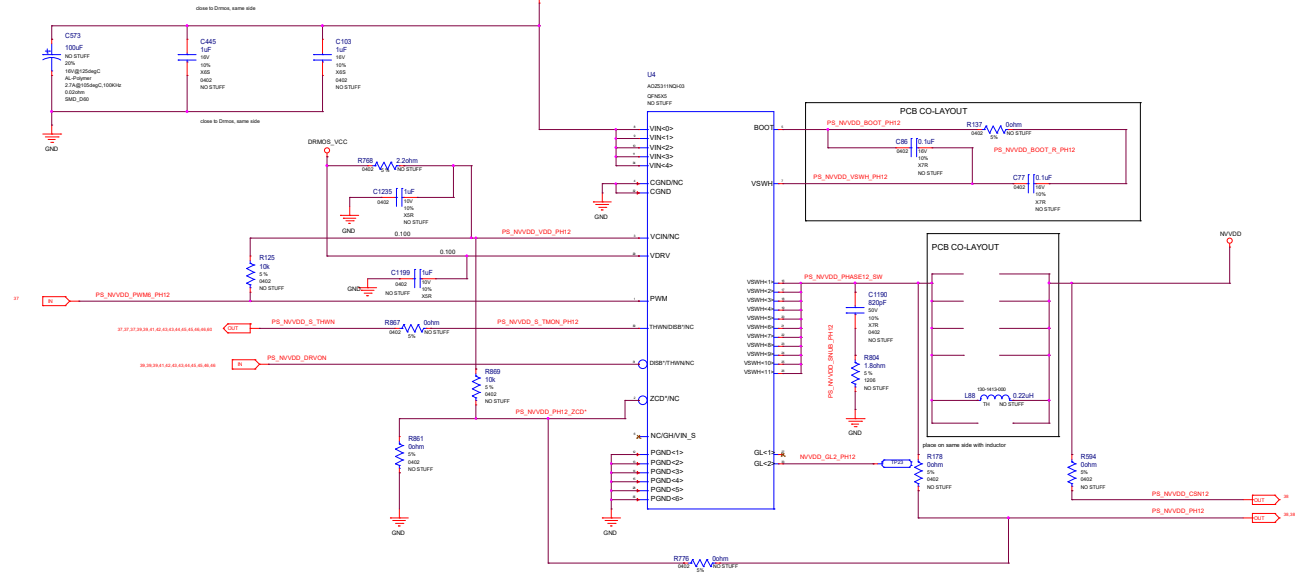
## NVVDD PH12

## NVVDD PH12(PWM6)

12V\_R2\_F\_NV



12V\_R2\_F\_NV



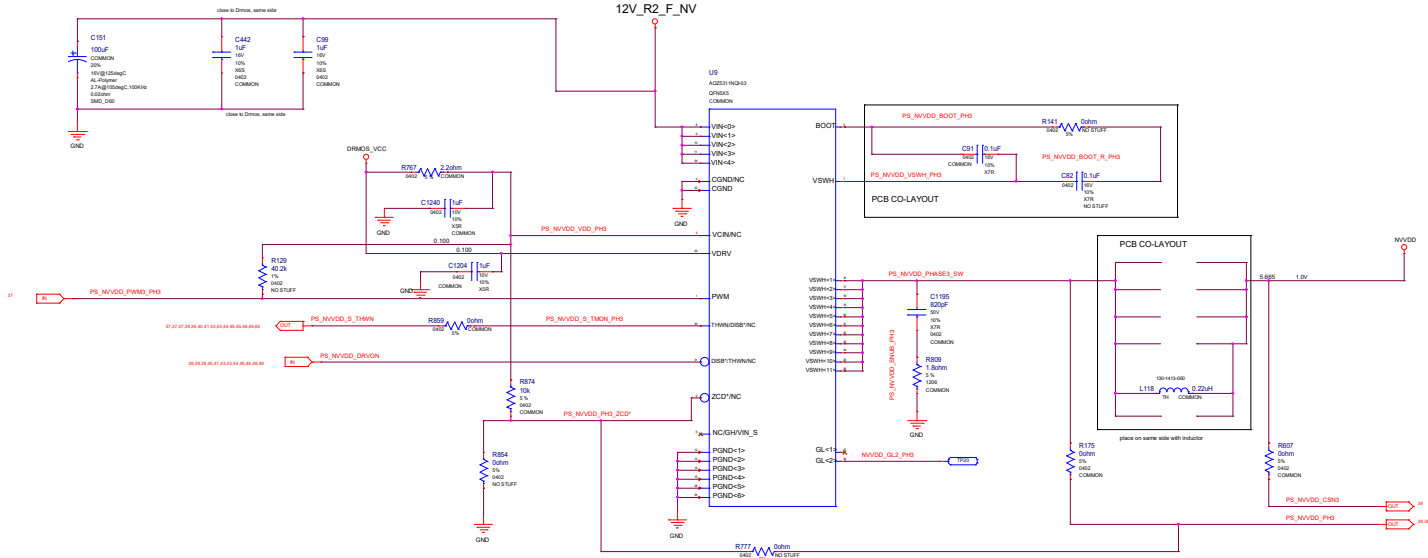
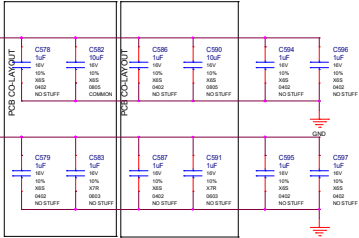




NVVDD PH3

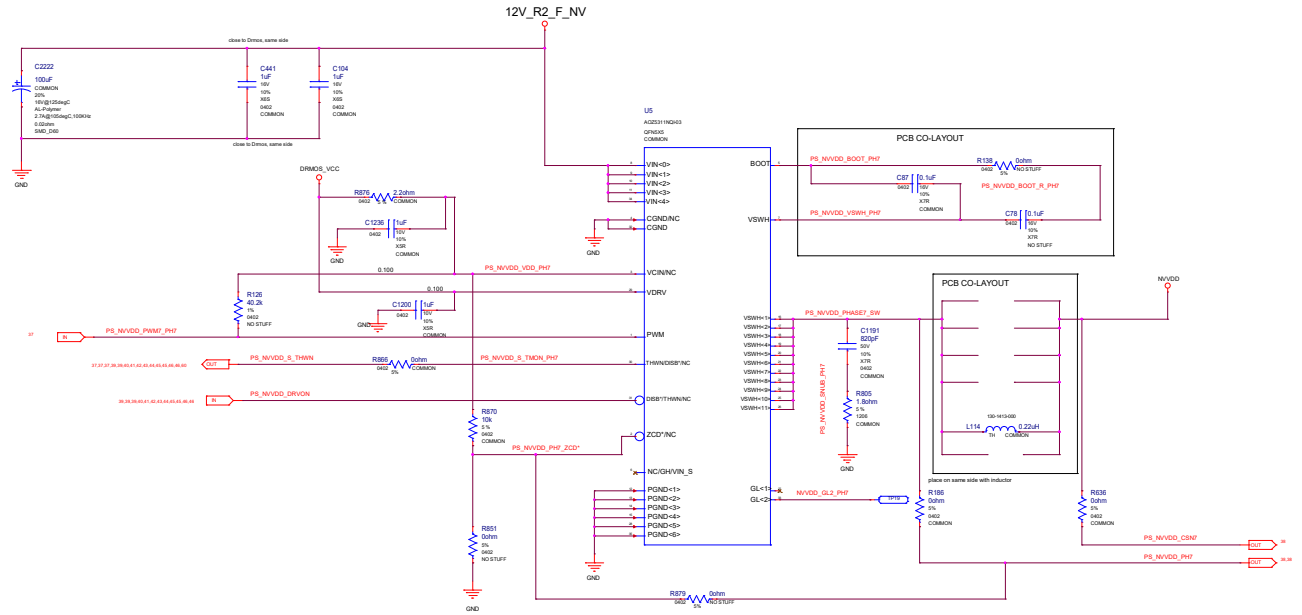
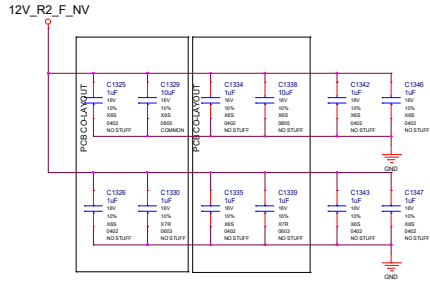
NVVDD PH3(PWM3)

12V\_R2\_F\_NV

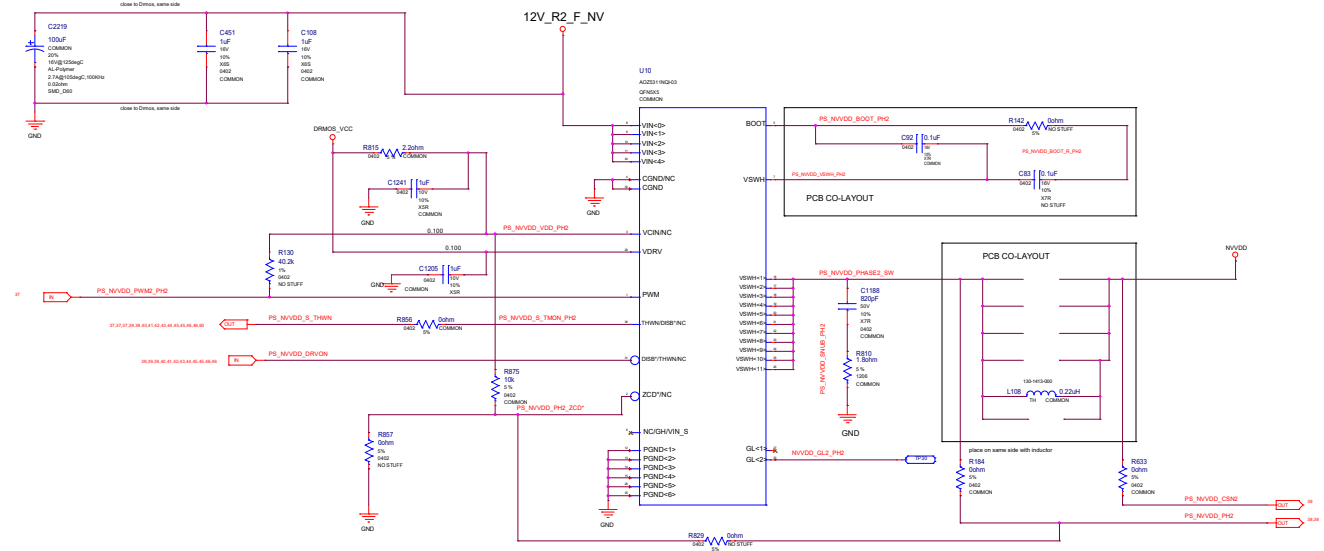
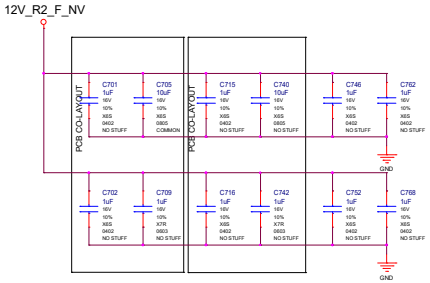


# NVDD PH2 & PH7

## NVDD PH7(PWM7)



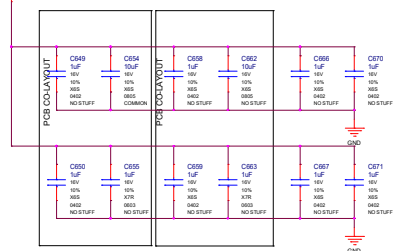
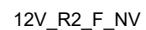
## NVDD PH2(PWM2)



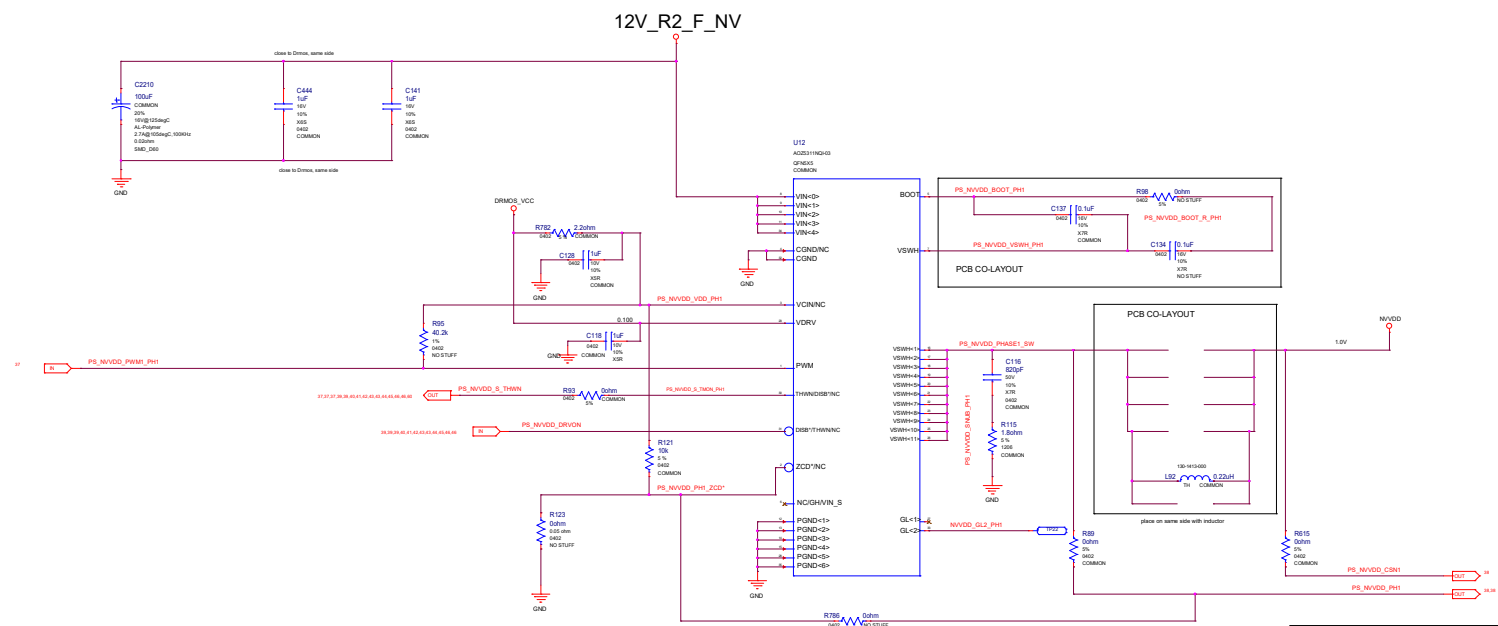
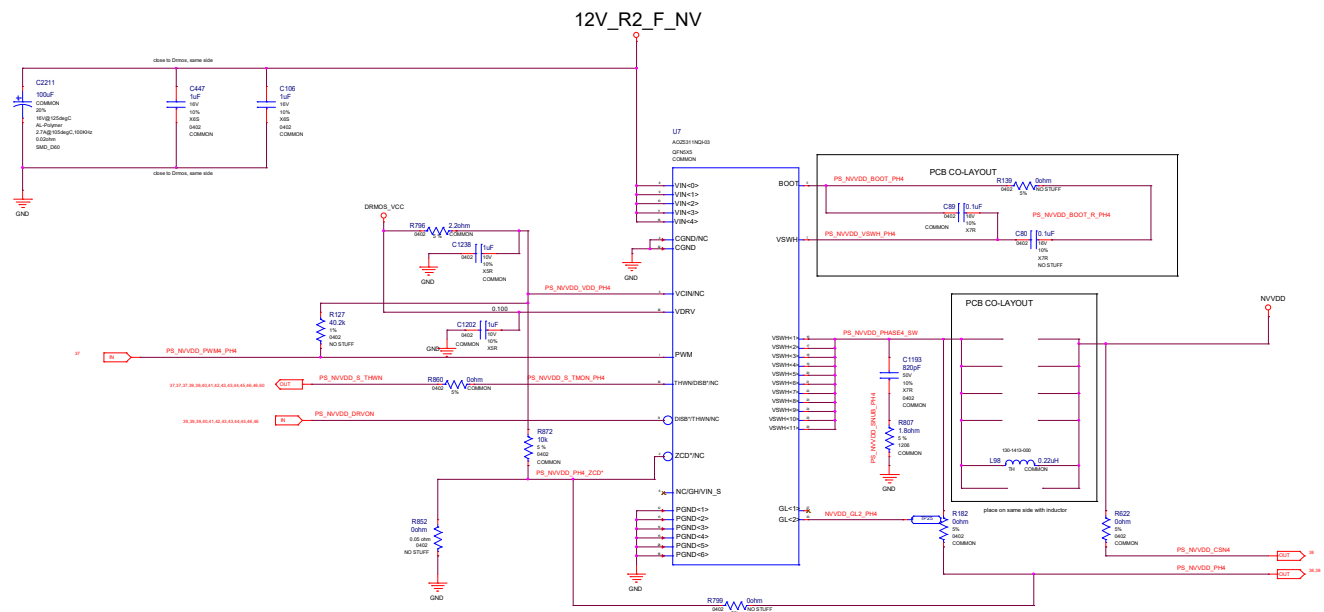
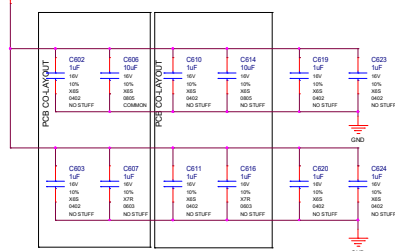
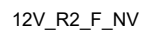


## NVVDD PH1 &amp; PH4

## NVVDD PH4(PWM4)

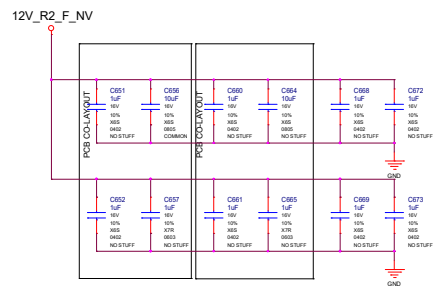


## NVVDD PH1(PWM1)

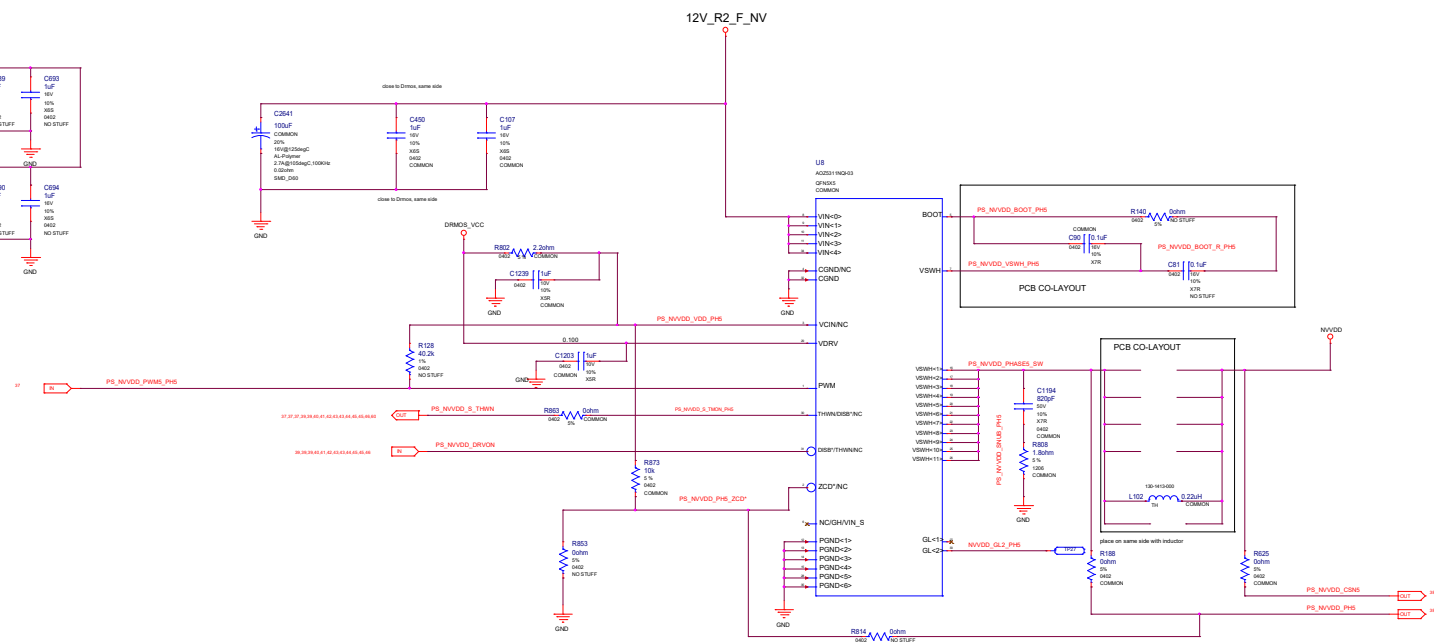
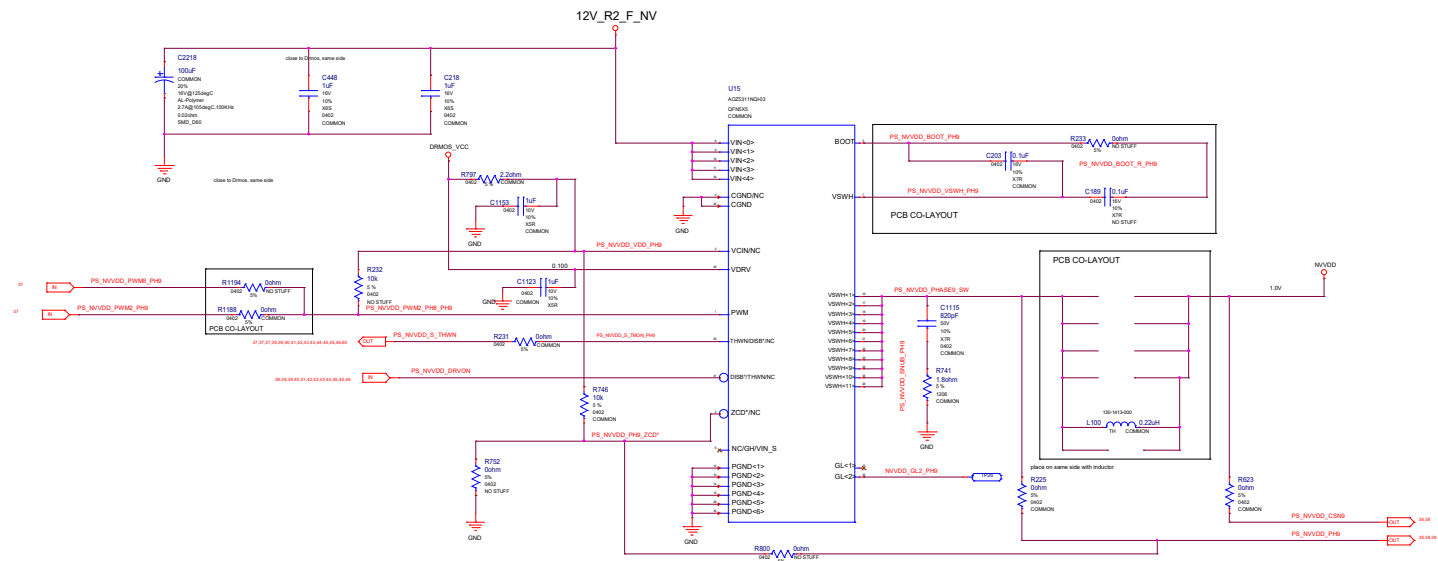
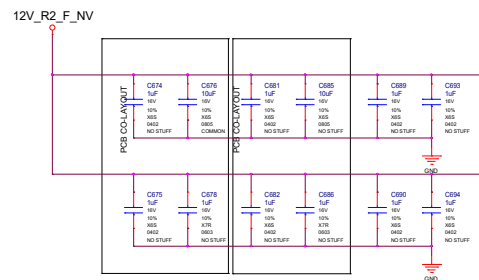


## NVVDD PH9 &amp; PH5

## NVVDD PH9(PWM2)

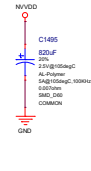
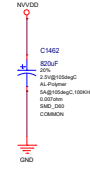


## NVVDD PH5(PWM5)

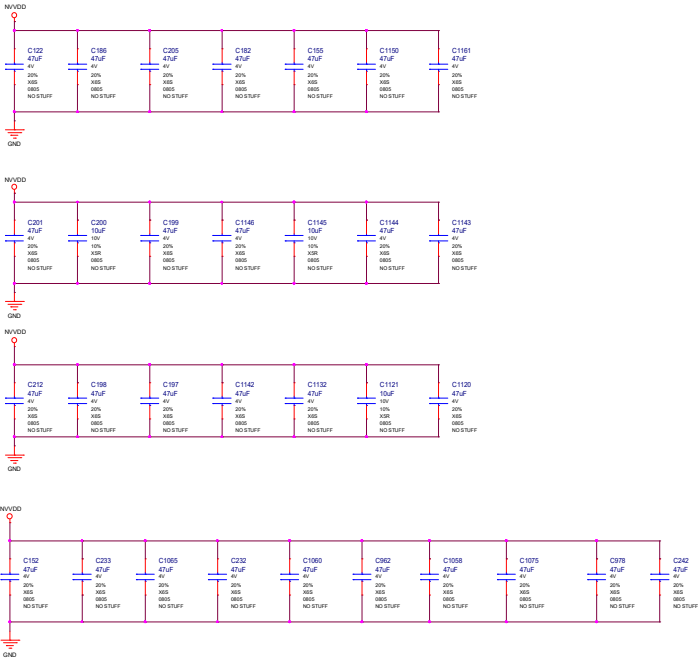


## NVVDD OUTPUT CAP 1

12xD60



NVDD OUTPUT CAP 2

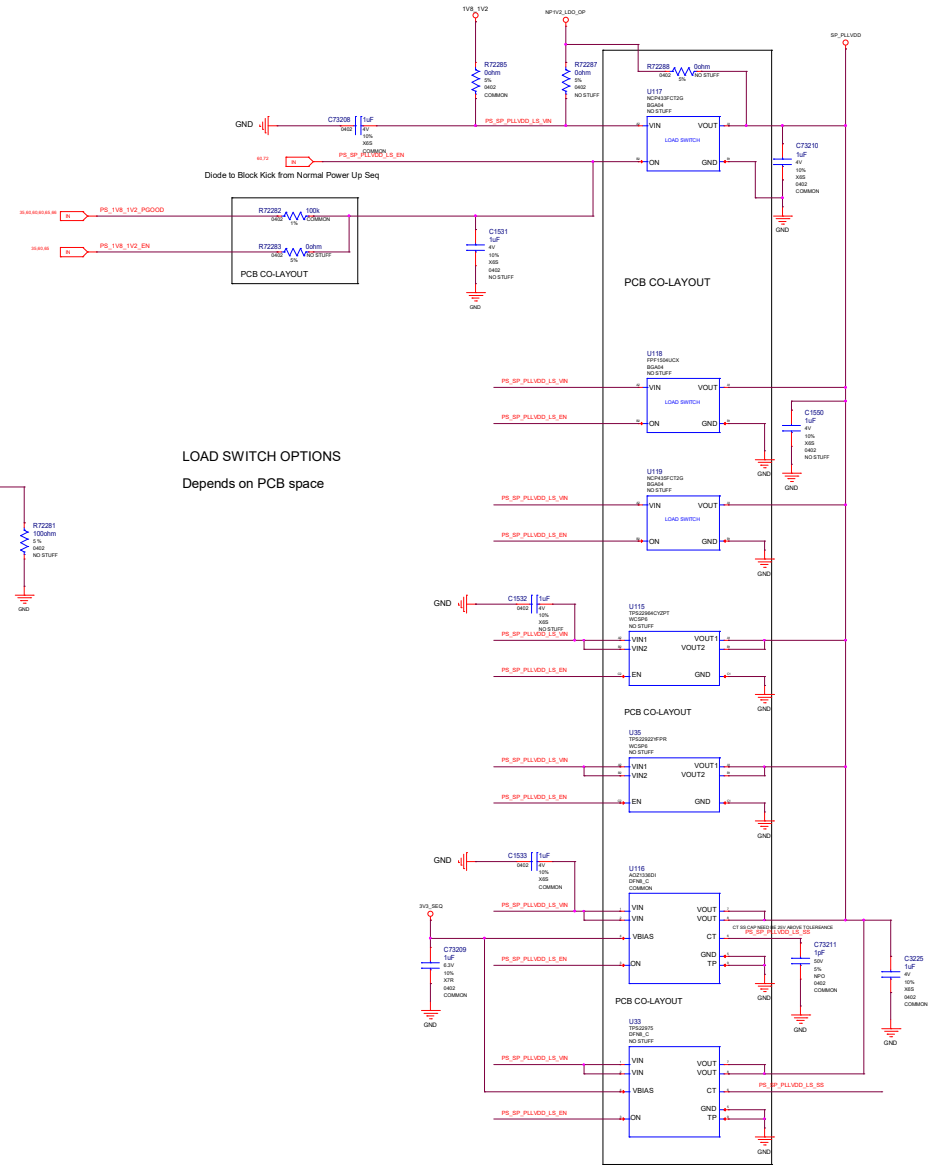
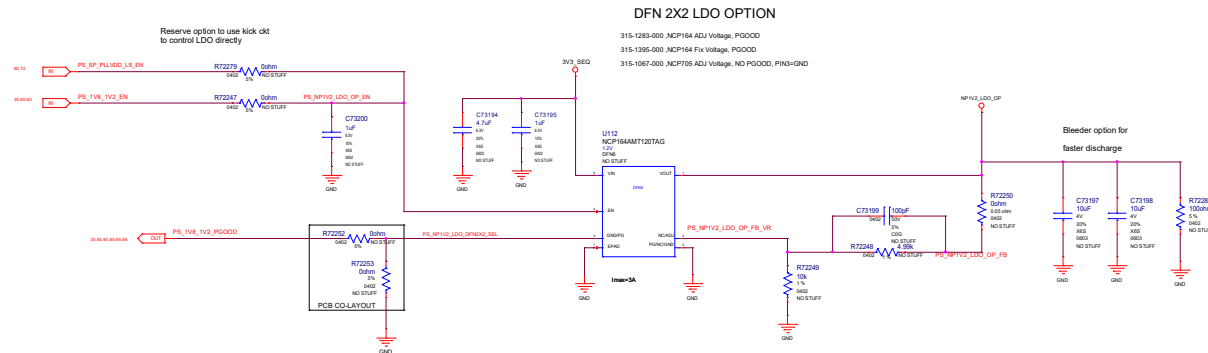




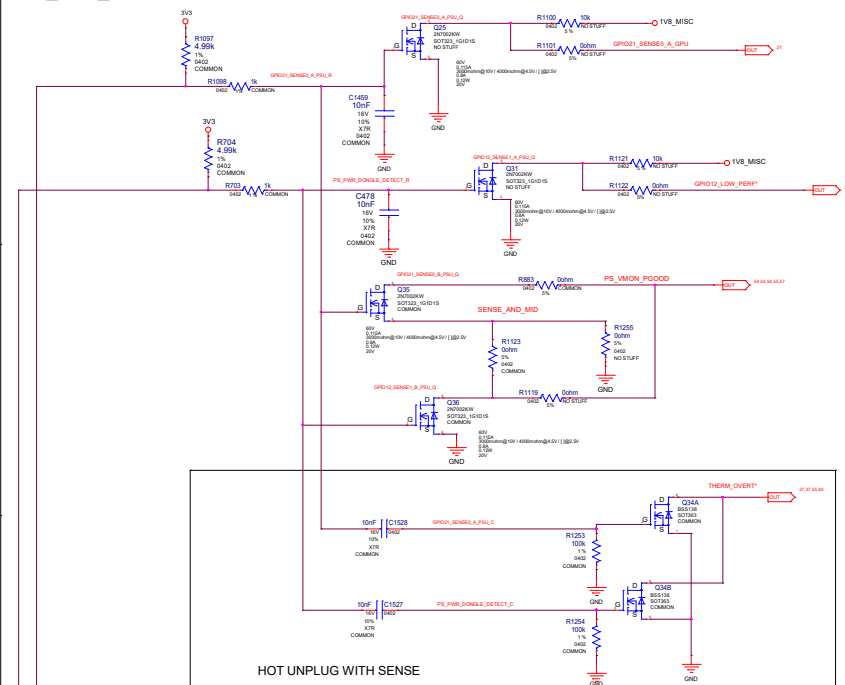
BLANK PAGE

BLANK PAGE

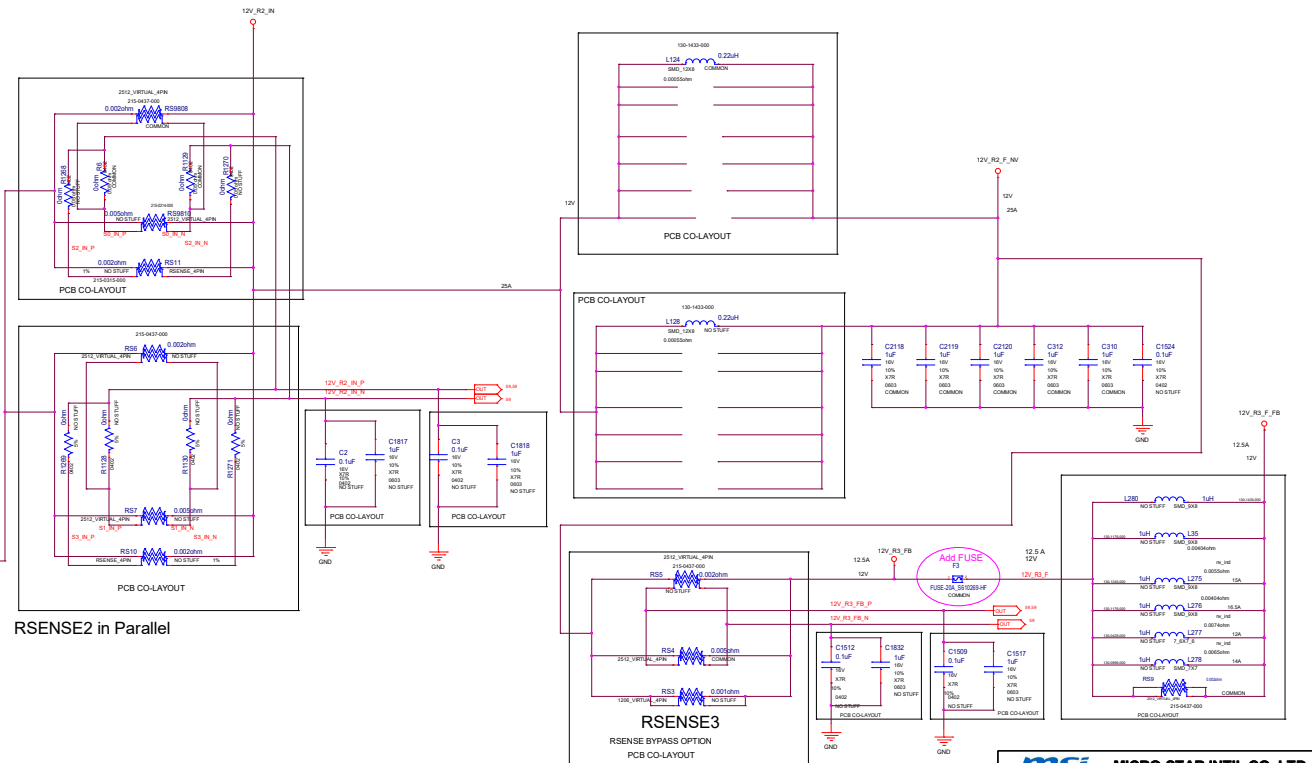
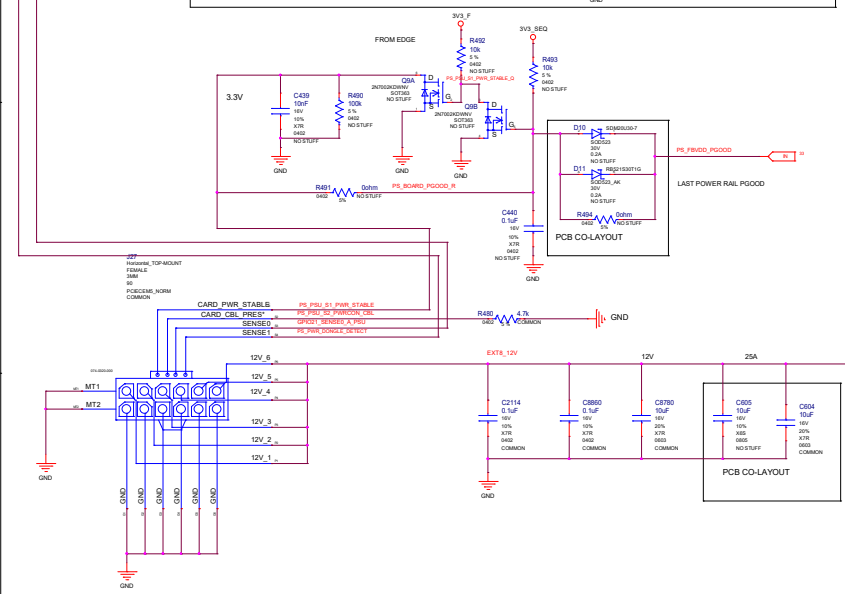
## SPPLLVDD\_LDO\_LOADSWITCH



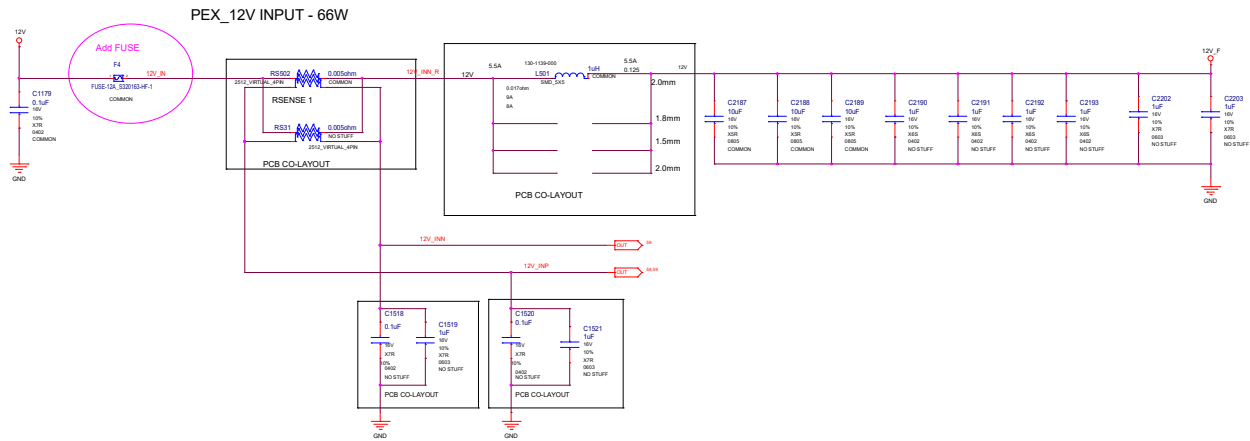
## 12V\_EXT\_INPUT, FILTERING



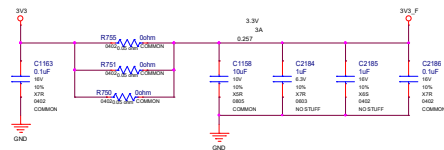
## HOT UNPLUG WITH SENSE



## PEX\_INPUT & FILTERING, PEX\_3V3

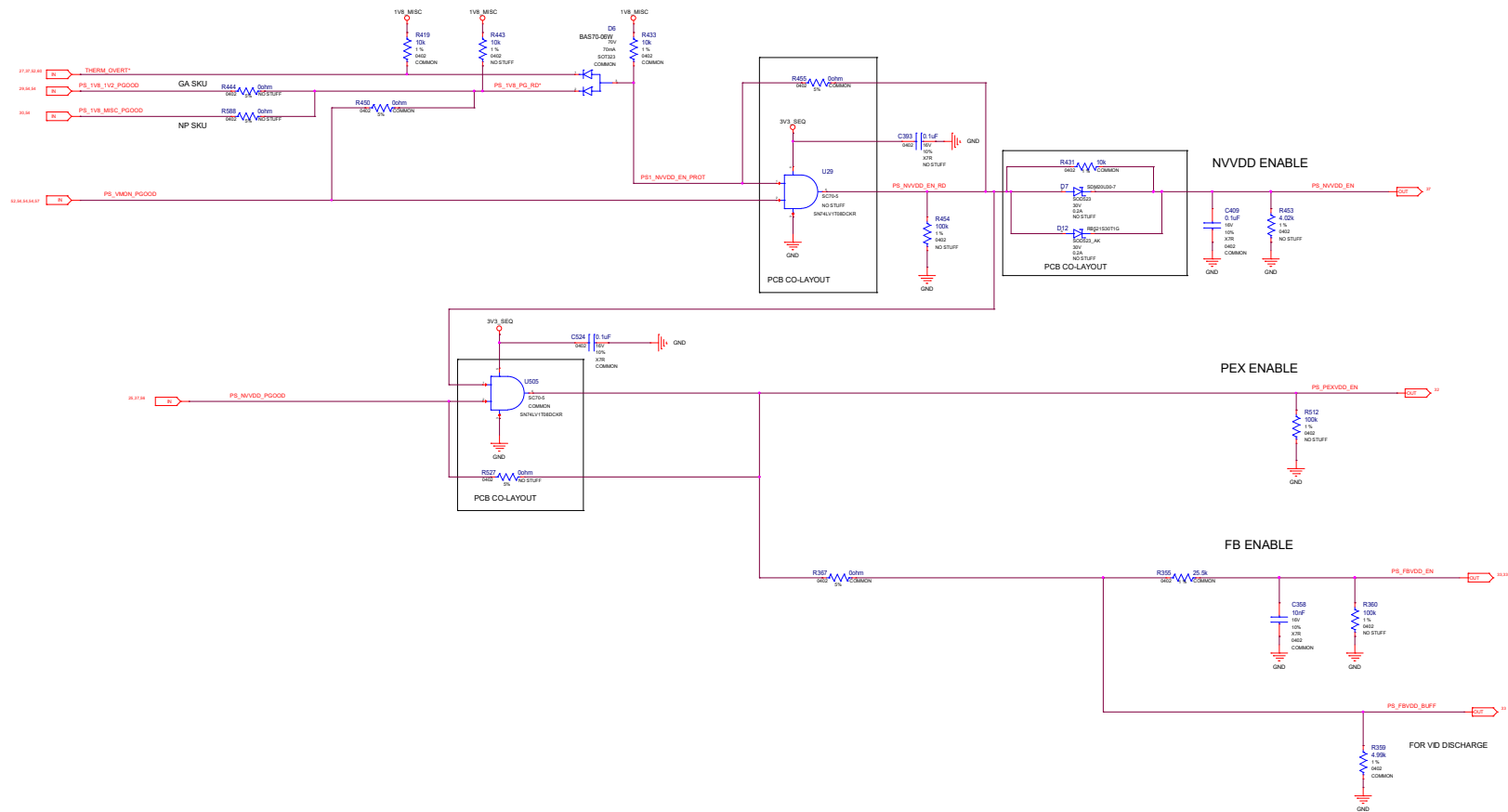


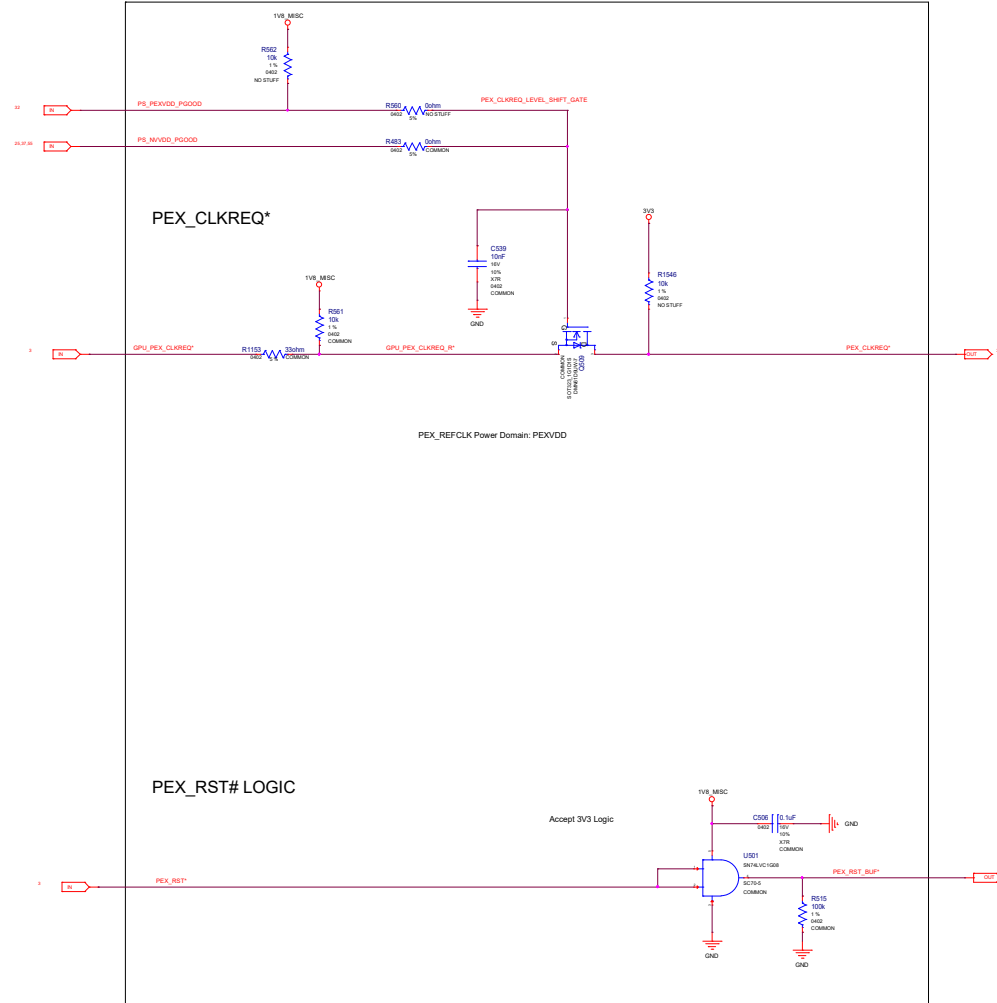
## PEX 3V3 INPUT - 10W





SEQ:NVVDD, PEX, FBVDDQ ENABLE







[illegible]

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence.Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOCK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

Remove 2-PIN LED HEADER FOR NORTH LOGO LED (WHITE)

DUAL FAN 4-PIN HEADERS



Copy from Y510-1.0


FAN B (RIGHT)

TV8 MSC



CNO

TV8 MSC



FAN A (LEFT)

Change in  $\Delta$  Susceptible:  $\Delta S_{\text{Susceptible}} = 1$ 

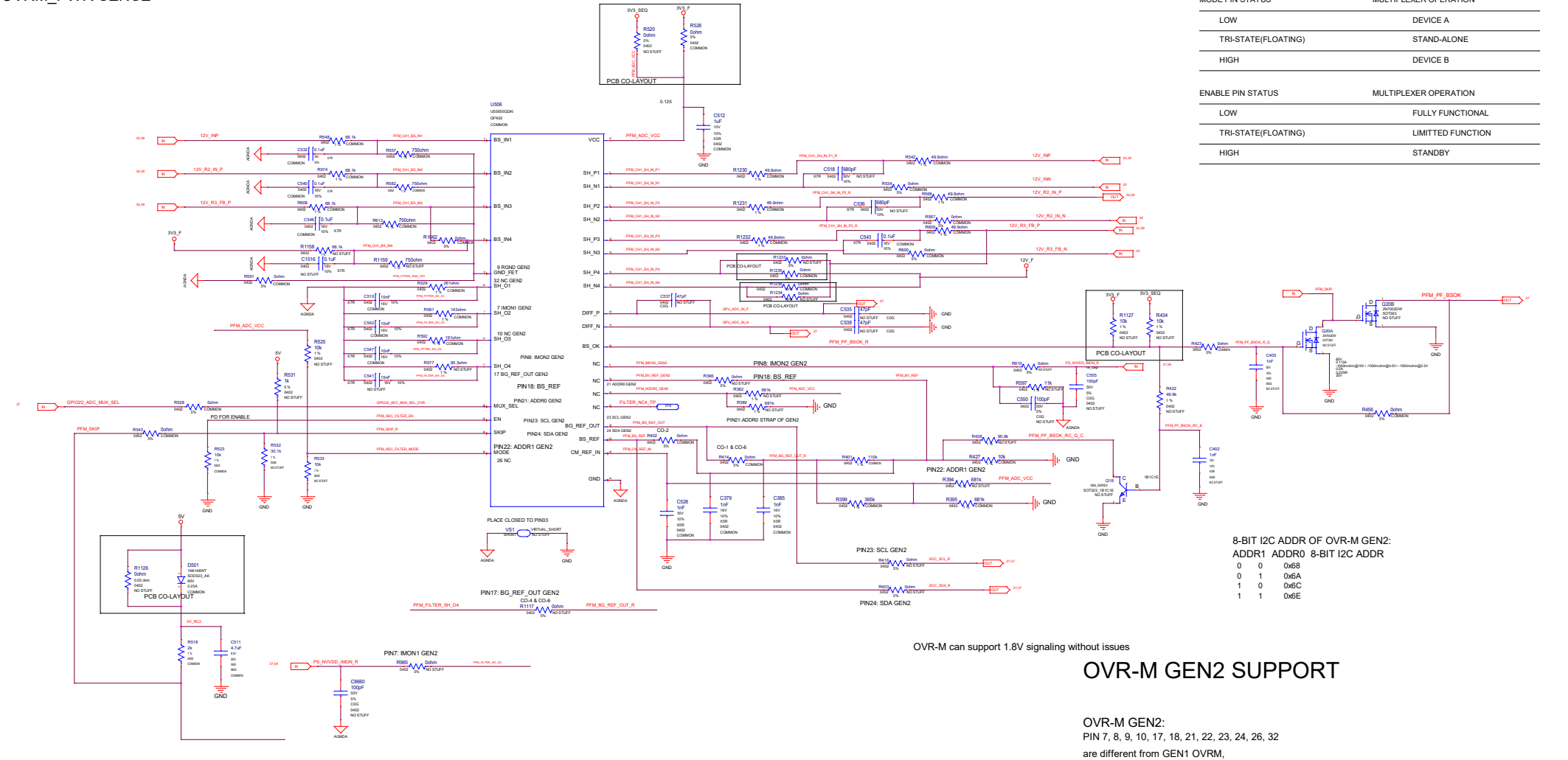
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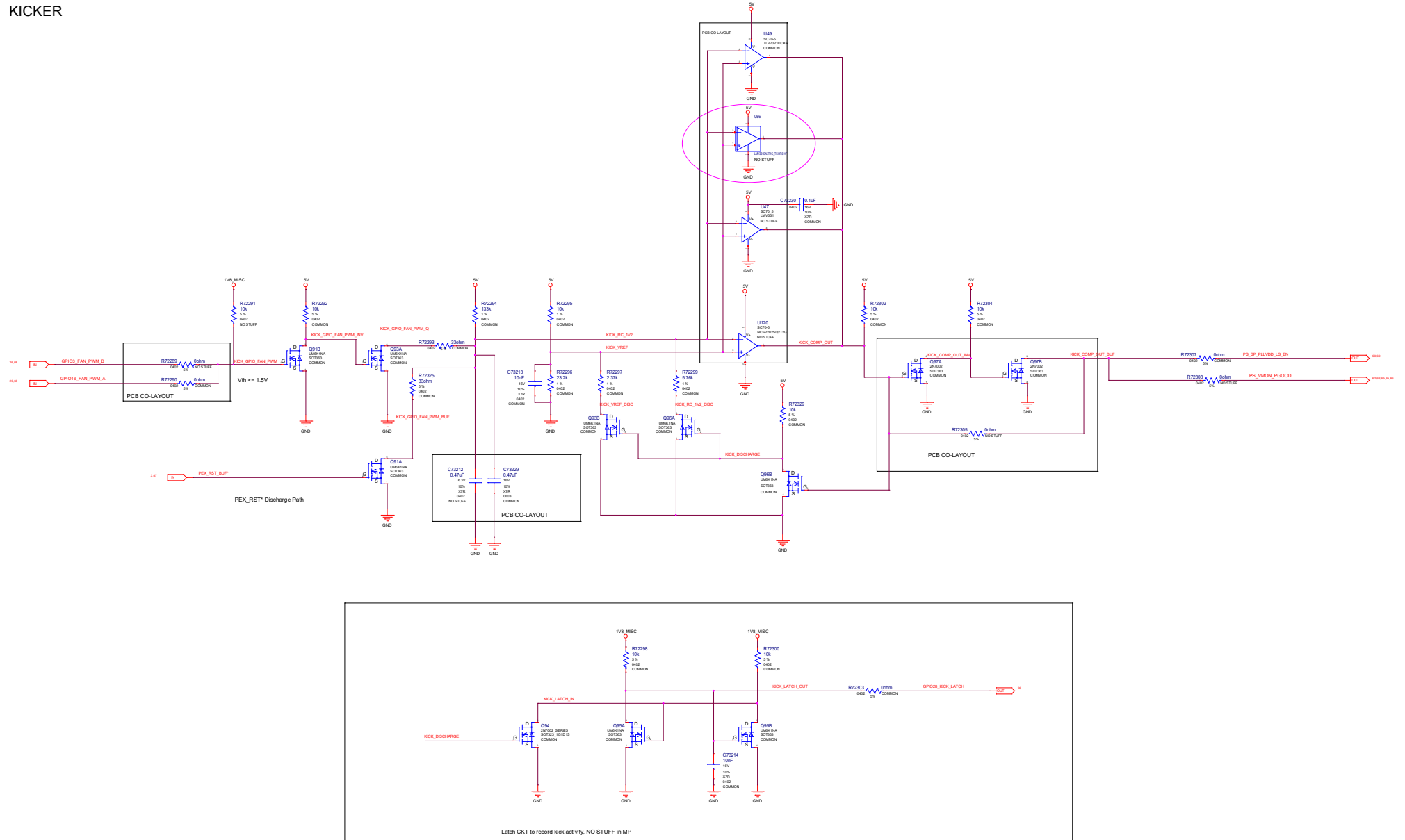
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OVRM\_PWR SENSE





KICKER



MOUNTING HOLES

